Stratix V Advanced Systems Development Board

Reference Manual

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1. Overview

This document describes the hardware features of the Stratix® V Advanced Systems development board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The development board comes with two Stratix V GX FPGA devices to provide a hardware platform for developing and prototyping high-performance and high-bandwidth application designs. The board includes a wide range of peripherals and memory interfaces to facilitate the development of Stratix V GX FPGA designs.

One FPGA Mezzanine Card (FMC) and one High-Speed Mezzanine Card (HSMC) connector is available to add additional functionality via a variety of FMC and HSMC cards available from both Altera and various partners.

Design advancements and innovations, such as the PCI Express hard IP implementation, partial reconfiguration, and programmable power technology ensure that designs implemented in the Stratix V GX FPGAs operate faster, with lower power than in previous FPGA families.

For more information on the following topics, refer to the respective documents or page:

- Stratix V device family, refer to the *Stratix V Device Handbook*.
- PCI Express hard IP implementation, refer to the *Stratix V Hard IP for PCI Express User Guide*.
- List of the latest daughter cards available, refer to the Development Board Daughtercards page of the Altera website.
- HSMC Specification, refer to the *High Speed Mezzanine Card (HSMC) Specification*.

Development Board Component Blocks

The board features the following major component blocks:

- Two Altera Stratix V FPGA (5SGXEA7N2F45C2N) in the 1932-pin FineLine BGA package
- MAX® V CPLD (5M2210ZF256C4N) System Controller in the 256-pin FineLine BGA package and Flash Fast Passive Parallel (FPP) configuration
  - 1-Gbit (Gb) serial flash
- FPGA Configuration Circuitry
  - MAX V CPLD (5M2210ZF256C4N) and FPP configuration.
  - On-Board USB-Blaster™ II for use with the Quartus® II Programmer, Nios® II Software Build Tools, and System Console.
  - EPCQ for x4 Active Serial (AS) configuration.
- On-Board Clocking Circuitry
  - 50-MHz, 100-MHz, and 125-MHz fully programmable oscillators
  - SMA connector for clock input (LVDS)
- General user input/output (I/O)
  - One eight-position dual in-line package (DIP) switch for each FPGA
  - 16 user LEDs for each FPGA
  - Three user push buttons for each FPGA
- Communication interfaces
  - One PCI Express x16 edge connector to PLX PE8747 Gen3 Switch
    - One PCI Express Gen3 x8 branch to each FPGA
  - One FMC connector (FPGA1)
  - One HSMC port (FPGA2)
  - One USB 2.0 on-board USB-Blaster II cable
- Power
  - 12-16 V (laptop) DC input
  - PCI Express edge connector
  - 2x4 PCI Express ATX connector
- System Monitoring
  - Power—voltage, current, wattage
  - Temperature—FPGA die, local board
- Mechanical
  - PCI Express full-length form factor
  - PCI Express chassis or bench-top operation

Dual FPGA

The development board includes two Stratix V GX FPGA devices that connect to other components on the board to provide a better transceiver and bandwidth design solution.

FPGA1

The first Stratix V GX FPGA device (FPGA1) connects to the following components:

- Communication interfaces
  - One Gen3 PCI Express x8 edge connector to PLX PEX8747 switch
  - One FPGA Mezzanine Card (FMC) port
- Memory interfaces
  - DDR3 SDRAM
    - Two 1024-MByte (MB) interfaces with 64-bit data bus
    - Two 512-MB interfaces with 32-bit data bus
  - Four 4.5-MB QDRII+ SRAM with 18-bit data bus
  - One 72-MB MoSys Bandwidth Engine IC SRAM with 16-bit data bus (16x10.3125 G XCVR)
  - One 32-MB serial flash
- General user I/O
  - LEDs
    - 16 user LEDs
    - Five PCI Express LEDs
    - Two FMC interface LEDs transmit/receive (TX/RX)
  - Push buttons and DIP switches
    - One CPU reset push button
    - Three general user push buttons
    - Eight general user DIP switches

FPGA2

The second Stratix V GX FPGA device (FPGA2) connects to the following components:

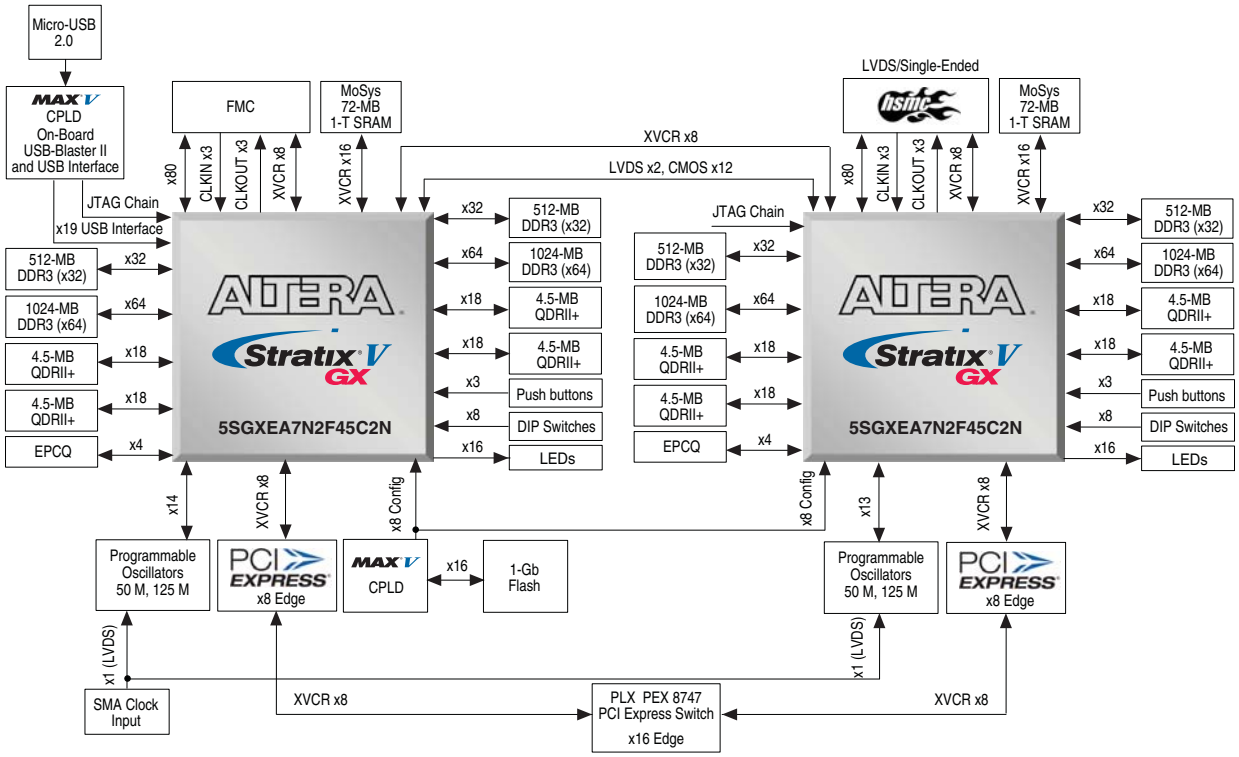
- Communication ports
  - One Gen3 PCI Express x8 edge connector to PLX PEX8747 switch
  - One universal HSMC port

- Memory interfaces
  - DDR3 SDRAM
    - Two 1024-MB interfaces with 64-bit data bus
    - Two 512-MB interfaces with 32-bit data bus
  - Four 4.5-MB QDRII+ SRAM with 18-bit data bus
  - One 72-MB MoSys Bandwidth Engine IC SRAM with 16-bit data bus (16x10.3125 G XCVR)
  - One 32-MB serial flash
- General user I/O
  - LEDs
    - 16 user LEDs
    - Two HSMC interface LEDs transmit/receive (TX/RX)
    - One PCI Express LEDs
  - Push buttons and DIP switches
    - One CPU reset push button
    - Three general user push buttons
    - Eight general user DIP switches

Development Board Block Diagram

Figure 1–1 shows the block diagram of the Stratix V Advanced Systems development board.

Figure 1–1. Stratix V Advanced Systems Development Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

This chapter introduces all the important components on the Stratix V Advanced Systems development board. Figure 2–1 illustrates major component locations and Table 2–1 provides a brief description of all features of the board.

A complete set of schematics, a physical layout database, and ODB++ files for the development board reside in the Stratix V Advanced Systems development kit **board_design_files** directory.

For information about powering up the board and installing the demo software, refer to the *Stratix V Advanced Systems Development Kit User Guide*.

This chapter consists of the following sections:

Board Overview

This section provides an overview of the Stratix V Advanced Systems development board, including an annotated board image and component descriptions. Figure 2–1 provides an overview of the development board features.

Figure 2–1. Overview of the Stratix V Advanced Systems Development Board Features

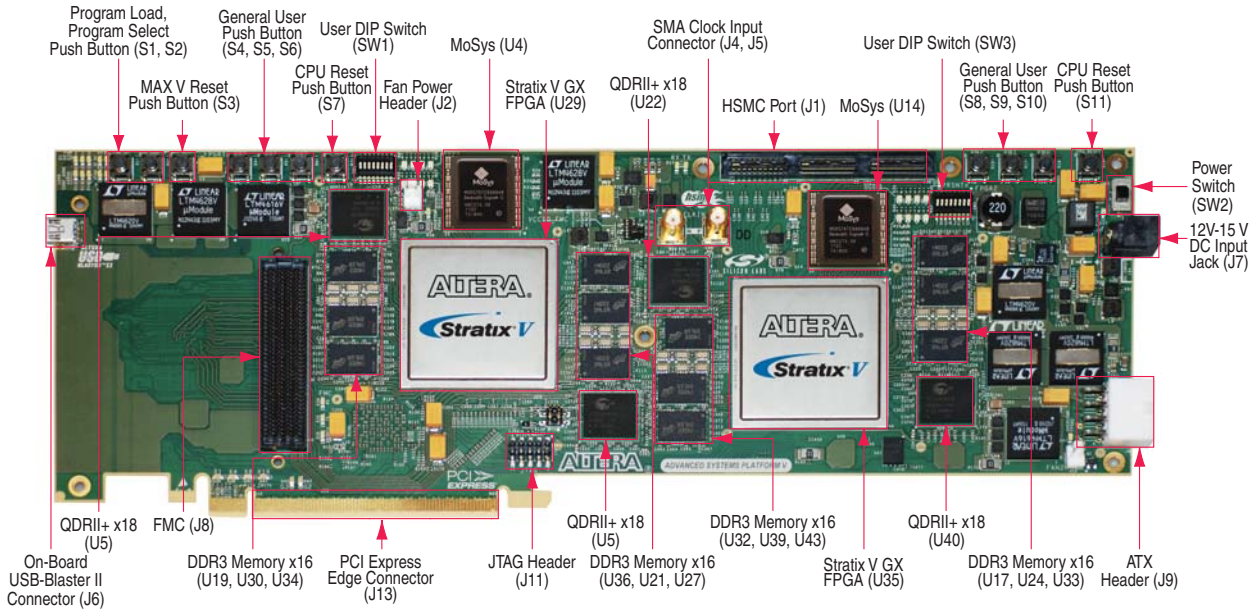


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Stratix V Advanced Systems Development Board Components (Part 1 of 4)

Board Reference	Type	Description
Featured Devices		
U29, U35	FPGA	5SGXEA7N2F45C2N, 1932-pin BGA.
U73	CPLD	5M2210ZF256C4, 256-pin BGA.
Configuration, Status, and Setup Elements		
J11	JTAG header	Provides access to the JTAG chain by using an external USB-Blaster cable (disables the on-board USB-Blaster II).
J6	On-Board USB-Blaster II	Mini-USB 2.0 connector for programming and debugging the FPGA.
SW7	JTAG DIP switch	Enables and disables devices in the JTAG chain. This switch is located on the back of the board.
SW5	FPGA1 mode select DIP switch	Sets the Stratix V (U29) `MSEL[2:0]` pins. FPGA1 `MSEL[4:3]` = 10 on the board.
SW6	FPGA2 mode select DIP switch	Sets the Stratix V (U35) `MSEL[2:0]` pins. FPGA2 `MSEL[4:3]` = 10 on the board.
SW4	Board settings DIP switch	Controls the MAX V CPLD System Controller functions such as clock select, clock enable, and FPP configuration control. This switch is located at the bottom of the board.

Table 2–1. Stratix V Advanced Systems Development Board Components (Part 2 of 4)

Board Reference	Type	Description
SW8	PCI Express DIP switch	Controls the PCI Express lane width by connecting the `prsnt` pins together on the PCI Express edge connector. This switch is located at the back of the board.
S1	Program select push button	Toggles the program LEDs, which selects the program image that loads from flash memory to the FPGAs.
S2	Program configuration push button	Configures the FPGAs from flash memory image based on the program LEDs.
D1, D2, D3	Program LEDs	Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when you press the program select push button.
D12	Load LED	Illuminates during FPGA configuration.
D13	Configuration done LED	Illuminates when the FPGA is configured.
D14	Error LED	Illuminates when the FPGA configuration from flash fails.
D27	Power LED	Illuminates when 5-V power is present.
D4, D5	System Console TX/RX LEDs	Indicate the transmit or receive activity of the System Console USB interface. The TX and RX LEDs would flicker if the link is in use and active. The LEDs are either off when not in use or on when in use but idle.
D15, D16	JTAG TX/RX LEDs	Indicate the transmit or receive activity of the JTAG chain. The TX and RX LEDs would flicker if the link is in use and active. The LEDs are either off when not in use or on when in use but idle.
D10, D11	HSMC TX/RX LEDs	You can configure these LEDs to indicate transmit or receive activity on the HSMC interface.
D21	HSMC Present LED	Illuminates when you plug a daughtercard into the HSMC connector.
D36	FMC Present LED	Illuminates when you plug a daughtercard into the FMC connector.
D42, D43	PCI Express Gen2/Gen3 LED	You can configure these LEDs to illuminate when PCI Express is in Gen2 or Gen3 mode.
D38, D39, D40, D41	PCI Express Link LEDs	You can configure these LEDs to display the PCI Express link width (x1, x4, x8, x16).
Clock Circuitry		
X1	125 M oscillator	125.000-MHz crystal oscillator for general purpose logic. A buffered copy of this clock is available on FPGA1 and FPGA2.
X2	50 M oscillator	50.000-MHz crystal oscillator for general purpose logic. A buffered copy of this clock is available on FPGA1, FPGA2, and MAX V CPLD.
U53	Quad-output oscillator	Programmable oscillator with default LVDS frequencies of 625 MHz, 206.25 MHz, 625 MHz, and 206.25 MHz.
U82	Quad-output oscillator	Programmable oscillator with default frequencies of 100 MHz (LVDS), 100 MHz (LVDS), 100 MHz (1.8-V CMOS), and 100 MHz (LVDS).
U95	Quad-output oscillator	Programmable oscillator with default LVDS frequencies of 100 MHz, 706.25 MHz, 206.25 MHz, and 206.25 MHz.
U100	Quad-output oscillator	Programmable oscillator with default frequencies of 100 MHz (LVDS), 100 MHz (LVDS), 100 MHz (1.8-V CMOS), and 100 MHz (LVDS).
X91	Quad-output oscillator	Programmable oscillator with default LVDS frequencies of 100 MHz, 644.53125 MHz, 644.53125 MHz, and 100 MHz.

Table 2–1. Stratix V Advanced Systems Development Board Components (Part 3 of 4)

Board Reference	Type	Description
X3	100 M oscillator	100-MHz crystal oscillator for the MAX V CPLD System Controller.
J4, J5	Clock input SMAs	Drives LVDS-compatible clock inputs into the clock multiplexer buffer.
General User Input and Output		
D6-D9, D17-D20, D22-D31	FPGA1 user LEDs	Two sets of eight bi-color LEDs (green and red) for 16 user LEDs for FPGA1. Illuminates when driven low.
D22-D25, D28-D31	FPGA2 user LEDs	Two sets of eight bi-color LEDs (green and red) for 16 user LEDs for FPGA2. Illuminates when driven low.
SW1	FPGA1 user DIP switch	Octal user DIP switch for FPGA1. When the switch is ON, a logic 0 is selected.
SW3	FPGA2 user DIP switch	Octal user DIP switch for FPGA2. When the switch is ON, a logic 0 is selected.
S3	MAX V reset push button	The default reset for the MAX V CPLD System Controller.
S7	FPGA1 CPU reset push button	The default reset for the FPGA1 logic.
S11	FPGA2 CPU reset push button	The default reset for the FPGA2 logic.
S4-S6	FPGA1 general user push button	Three user push buttons for FPGA1. Driven low when pressed.
S8-S10	FPGA2 general user push button	Three user push buttons for FPGA2. Driven low when pressed.
Memory Devices		
U19, U57	DDR3A x32	512-MB DDR3 x64-bit data bus interfacing to FPGA1, consisting of two x16-bit devices with a single address and command bus.
U30, U34, U72, U80	DDR3B x64	1024-MB DDR3 x64-bit data bus interfacing to FPGA1, consisting of four x16-bit devices with a single address and command bus.
U36, U81	DDR3C x32	512-MB DDR3 x64-bit data bus interfacing to FPGA1, consisting of two x16-bit devices with a single address and command bus.
U21, U27, U58, U68	DDR3D x64	1024-MB DDR3 x64-bit data bus interfacing to FPGA1, consisting of four x16-bit devices with a single address and command bus.
U32, U75,	DDR3E x32	512-MB DDR3 x64-bit data bus interfacing to FPGA2, consisting of two x16-bit devices with a single address and command bus.
U39, U43, U88, U92	DDR3F x64	1024-MB DDR3 x64-bit data bus interfacing to FPGA2, consisting of four x16-bit devices with a single address and command bus.
U33, U78	DDR3G x32	512-MB DDR3 x64-bit data bus interfacing to FPGA2, consisting of two x16-bit devices with a single address and command bus.
U17, U24, U55, U64	DDR3H x64	1024-MB DDR3 x64-bit data bus interfacing to FPGA2, consisting of four x16-bit devices with a single address and command bus.
U12, U52, U41, U90	QDRII+ x18 (interfaces A to D)	Four 4.5-MB QDRII+ SRAM interfaces with a 18-bit data bus for FPGA1. The device has a separate 18-bit read and 18-bit write port with DDR signalling at up to 533 MHz.
U22, U61, U40, U89	QDRII+ x18 (interfaces E to H)	Four 4.5-MB QDRII+ SRAM interfaces with a 18-bit data bus for FPGA2. The device has a separate 18-bit read and 18-bit write port with DDR signalling at up to 533 MHz.
U4	MoSys x16	A 72-MB MoSys Bandwidth Engine IC SRAM with a 16-bit transceiver data bus for FPGA1.

Table 2–1. Stratix V Advanced Systems Development Board Components (Part 4 of 4)

Board Reference	Type	Description
U14	MoSys x16	A 72-MB MoSys Bandwidth Engine IC SRAM with a 16-bit transceiver data bus for FPGA2.
U86	Flash x16	A 1-Gb synchronous flash device with a 16-bit data bus for non-volatile memory. Only accessible from the MAX V System Controller, intended for FPGA configuration.
U93, U48	EPCQ x4	A 32-MB serial flash is available for each FPGA to use during active serial (AS) configuration.
U76, U83	EEPROM	A single 8-Kbit serial EEPROM is available for each FPGA to store board information.
Communication Ports		
J13	PCI Express edge connector	Made of gold-plated edge fingers for up to ×16 signaling in either Gen1, Gen2, or Gen3 mode.
U47	PLX PCI Express switch	Switch x16 PCI Express data between FPGA1 x8 and FPGA2 x8 via the PEX8747 PCIe switch.
J8	FMC port	Provides 10 transceiver channels and 74 CMOS or 17 LVDS channels.
J1	HSMC port	Provides eight transceiver channels and 84 CMOS or 17 LVDS channels.
Power Supply		
J13	PCI Express edge connector	Interfaces to a PCI Express root port such as an appropriate PC motherboard.
J10	PCI Express 2x4 ATX power	PCI Express compliant 2x4 auxiliary power connector. This can supply an additional 150 W to the board.
J7	DC input jack	Accepts a 12- to 15-V DC power supply.
SW2	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

Featured Device: Stratix V GX FPGA

The Stratix V Advanced Systems development board features two Stratix V GX FPGA 5SGXEA7N2F45C2N devices (U29, U35) in a 1932-pin FineLine BGA package.

For more information about the Stratix V device family, refer to the *Stratix V Device Handbook*.

Table 2–2 describes the features of the Stratix V GX FPGA 5SGXEA7N2F45C2N device.

Table 2–2. Stratix V GX FPGA 5SGXEA7N2F45C2N Features

ALMs	Equivalent LEs	Registers	M20K Memory (Mb)	18-bit × 18-bit Multipliers	Fractional PLLs	Transceiver Channels (12.5 Gbps)	Package Type
358,500	622,000	939,000	50	512	28	48	1932-pin FineLine BGA

I/O Resources

Table 2–3 lists the Stratix V GX FPGA device pin count and usage by function on the development board.

Table 2–3. Stratix V GX FPGA Pin Count and Usage (Part 1 of 2)

Function	I/O Standard	I/O Count	Special Pins
FPGA1			
DDR3	1.5-V SSTL	368	4 differential, 24 differential DQS
QDRII+	1.5-V SSTL	260	4 differential DQS
EEPROM	2.5-V CMOS	2	
FMC	Adjustable	80	36 differential, 2 reference clocks
Switches	1.5-V CMOS	8	
LEDs	1.5-V/2.5-V CMOS	19	
Push buttons	1.5-V/2.5-V CMOS	4	
Chip-to-chip	2.5-V CMOS + LVDS	20	4 differential
MAX V Interface	1.5-V/2.5-V CMOS	4	
MoSys	1.5-V CMOS	10	
PCI Express/PLX	1.5-V/2.5-V CMOS	10	
Clocks or Oscillators	1.5-V CMOS + LVDS	26	5 differential clock, 7 differential reference clocks
On-board USB-Blaster II	1.5-V CMOS	19	
Total I/O Used:		**830**	
Transceiver Pairs			
Chip-to-chip		8	
FMC		10	
MoSys		16	
PCI Express/PLX		8	
Total Transceivers Used:		**42**	
FPGA2			
DDR3	1.5-V SSTL	368	4 differential, 24 differential DQS
QDRII+	1.5-V SSTL	260	4 differential DQS
EEPROM	2.5-V CMOS	2	
HSMC	2.5-V CMOS + LVDS	84	38 differential, 3 clocks
Switches	1.5-V CMOS	8	
LEDs	1.5-V CMOS	19	
Push-buttons	1.5-V/2.5-V CMOS	4	
Chip-to-chip	2.5-V CMOS + LVDS	20	4 differential
MAX V Interface	1.5-V/2.5-V CMOS	4	
MoSys	1.5-V CMOS	10	
PCI Express/PLX	1.5-V/2.5-V CMOS	6	
Clocks or Oscillators	1.5-V CMOS + LVDS	24	5 differential clock, 6 differential reference clocks
Total I/O Used:		**809**	

Table 2–3. Stratix V GX FPGA Pin Count and Usage (Part 2 of 2)

Function	I/O Standard	I/O Count	Special Pins
Transceiver Pairs			
Chip-to-chip		8	
HSMC		8	
MoSys		16	
PCI Express/PLX		8	
Total Transceivers Used:		**40**	

MAX V CPLD System Controller

The board utilizes the 5M2210ZF256C4 System Controller, an Altera MAX V CPLD, for the following purposes:

- FPGA configuration from flash memory
- Power consumption monitoring
- Temperature monitoring
- Fan control
- Control registers for clocks
- Control registers for remote system update

Figure 2–2 illustrates the MAX V CPLD System Controller's functionality and external circuit connections as a block diagram.

Figure 2–2. MAX V CPLD System Controller Block Diagram

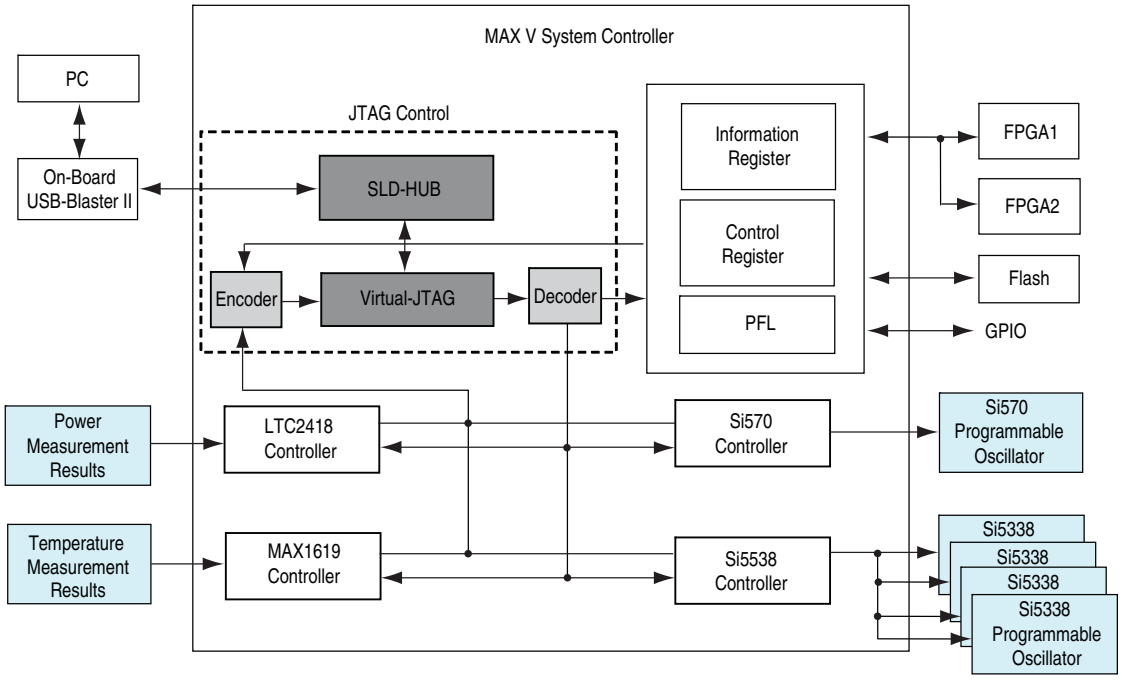


Table 2–4 lists the I/O signals present on the MAX V CPLD System Controller. The signal names and functions are relative to the MAX V device (U73).

Table 2–4. MAX V CPLD System Controller Device Pin-Out (Part 1 of 5)

Schematic Signal Name	MAX V CPLD Pin Number	I/O Standard	Description
CLK125_EN	A2	2.5-V	125 MHz oscillator enable
CLK50_EN	E9	2.5-V	50 MHz oscillator enable
CLK_CONFIG	J5	2.5-V	100 MHz configuration clock input
CLK_ENABLE	C13	2.5-V	DIP switch for clock oscillator enable
CLK_SEL	D11	2.5-V	DIP switch for clock select SMA or oscillator
CLOCK_SCL	M2	2.5-V	Programmable oscillator I^2C clock
CLOCK_SDA	M3	2.5-V	Programmable oscillator I^2C data
FACTORY_LOAD	B13	2.5-V	DIP switch to load factory image from flash at power-up
FACTORY_REQUEST	R14	1.5-V	On-Board USB-Blaster II request to send factory command
FACTORY_STATUS	N12	1.5-V	On-Board USB-Blaster II factory command status
FLASH_ADVN	K12	1.8-V	FM bus flash memory address valid
FLASH_CEN	D13	1.8-V	FM bus flash memory chip enable
FLASH_CLK	F12	1.8-V	FM bus flash memory clock
FLASH_OEN	D14	1.8-V	FM bus flash memory output enable
FLASH_RDYBSYN	F11	1.8-V	FM bus flash memory chip ready 0
FLASH_RESETN	P14	1.8-V	FM bus flash memory reset
FLASH_WEN	K13	1.8-V	FM bus flash memory write enable
FLASH_WPN	M14	1.8-V	FM bus flash memory write protect
FLASH_A1	C14	1.8-V	FM address bus
FLASH_A2	C15	1.8-V	FM address bus
FLASH_A3	E13	1.8-V	FM address bus
FLASH_A4	E12	1.8-V	FM address bus
FLASH_A5	D15	1.8-V	FM address bus
FLASH_A6	F14	1.8-V	FM address bus
FLASH_A7	D16	1.8-V	FM address bus
FLASH_A8	F13	1.8-V	FM address bus
FLASH_A9	E15	1.8-V	FM address bus
FLASH_A10	E16	1.8-V	FM address bus
FLASH_A11	F15	1.8-V	FM address bus
FLASH_A12	G14	1.8-V	FM address bus
FLASH_A13	F16	1.8-V	FM address bus
FLASH_A14	G13	1.8-V	FM address bus
FLASH_A15	N16	1.8-V	FM address bus
FLASH_A16	G12	1.8-V	FM address bus
FLASH_A17	G16	1.8-V	FM address bus
FLASH_A18	H14	1.8-V	FM address bus

Table 2–4. MAX V CPLD System Controller Device Pin-Out (Part 2 of 5)

Schematic Signal Name	MAX V CPLD Pin Number	I/O Standard	Description
FLASH_A19	H15	1.8-V	FM address bus
FLASH_A20	H13	1.8-V	FM address bus
FLASH_A21	H16	1.8-V	FM address bus
FLASH_A22	J13	1.8-V	FM address bus
FLASH_A23	J16	1.8-V	FM address bus
FLASH_A24	G15	1.8-V	FM address bus
FLASH_A25	L16	1.8-V	FM address bus
FLASH_A26	E14	1.8-V	FM address bus
FLASH_D0	J14	1.8-V	FM data bus
FLASH_D1	J15	1.8-V	FM data bus
FLASH_D2	K16	1.8-V	FM data bus
FLASH_D3	N15	1.8-V	FM data bus
FLASH_D4	K15	1.8-V	FM data bus
FLASH_D5	N14	1.8-V	FM data bus
FLASH_D6	L14	1.8-V	FM data bus
FLASH_D7	L11	1.8-V	FM data bus
FLASH_D8	L15	1.8-V	FM data bus
FLASH_D9	L12	1.8-V	FM data bus
FLASH_D10	M16	1.8-V	FM data bus
FLASH_D11	L13	1.8-V	FM data bus
FLASH_D12	M15	1.8-V	FM data bus
FLASH_D13	M13	1.8-V	FM data bus
FLASH_D14	K14	1.8-V	FM data bus
FLASH_D15	P15	1.8-V	FM data bus
FMC_C2M_PG	E3	2.5-V	FMC carrier card to mezzanine module power good
FPGA1_CONF_DONE	A13	2.5-V	FPGA1 configuration done
FPGA1_CPU_RESETN	B1	2.5-V	FPGA1 reset
FPGA1_CVP_CONFDONE	N10	1.5-V	FPGA1 configuration via protocol done
FPGA1_DCLK	J3	2.5-V	FPGA1 configuration clock
FPGA1_FPP	A15	2.5-V	Configure FPGA1 via FPP at power up
FPGA1_MSEL0	A7	2.5-V	DIP switch for FPGA1 mode select 0
FPGA1_MSEL1	E1	2.5-V	DIP switch for FPGA1 mode select 1
FPGA1_MSEL2	A6	2.5-V	DIP switch for FPGA1 mode select 2
FPGA1_MSEL3	A12	2.5-V	FPGA1 mode select 3
FPGA1_MSEL4	A5	2.5-V	FPGA1 mode select 4
FPGA1_NCE	B3	2.5-V	FPGA1 chip enable
FPGA1_NCEO	F1	2.5-V	FPGA1 chip enable output
FPGA1_NCONFIG	K2	2.5-V	FPGA1 configuration active
FPGA1_NSTATUS	J4	2.5-V	FPGA1 configuration ready status

Table 2–4. MAX V CPLD System Controller Device Pin-Out (Part 3 of 5)

Schematic Signal Name	MAX V CPLD Pin Number	I/O Standard	Description
FPGA1_OVERTEMP	A11	2.5-V	FPGA1 temperature monitor fan enable
FPGA1_OVERTEMPN	D7	2.5-V	FPGA1 temperature monitor over-temperature indicator LED
FPGA1_PR_DONE	N9	1.5-V	FPGA1 partial reconfiguration done
FPGA1_PR_ERROR	M10	1.5-V	FPGA1 partial reconfiguration error
FPGA1_PR_READY	M8	1.5-V	FPGA1 partial reconfiguration ready
FPGA1_PR_REQUEST	R3	1.5-V	FPGA1 partial reconfiguration request
FPGA2_CONF_DONE	P2	2.5-V	FPGA2 configuration done
FPGA2_CPU_RESETN	N3	2.5-V	FPGA2 reset
FPGA2_CVP_CONFDONE	T2	2.5-V	FPGA2 configuration via protocol done
FPGA2_DCLK	K5	2.5-V	FPGA2 configuration clock
FPGA2_FPP	B14	2.5-V	Configure FPGA2 via FPP at power up
FPGA2_MSEL0	G1	2.5-V	DIP switch for FPGA2 mode select 0
FPGA2_MSEL1	L1	2.5-V	DIP switch for FPGA2 mode select 1
FPGA2_MSEL2	J1	2.5-V	DIP switch for FPGA2 mode select 2
FPGA2_MSEL3	N1	2.5-V	FPGA2 mode select 3
FPGA2_MSEL4	M1	2.5-V	FPGA2 mode select 4
FPGA2_NCE	K1	2.5-V	FPGA2 chip enable
FPGA2_NCEO	M4	2.5-V	FPGA2 chip enable output
FPGA2_NCONFIG	L5	2.5-V	FPGA2 configuration active
FPGA2_NSTATUS	H1	2.5-V	FPGA2 configuration ready status
FPGA2_OVERTEMP	D10	2.5-V	FPGA2 temperature monitor fan enable
FPGA2_OVERTEMPN	E10	2.5-V	FPGA2 temperature monitor over-temperature indicator LED
FPGA2_PR_DONE	R6	1.5-V	FPGA2 partial reconfiguration done
FPGA2_PR_ERROR	R1	1.5-V	FPGA2 partial reconfiguration error
FPGA2_PR_READY	T5	1.5-V	FPGA2 partial reconfiguration ready
FPGA2_PR_REQUEST	R5	1.5-V	FPGA2 partial reconfiguration request
FPGA_CONFIG_D0	D3	2.5-V	FPGA configuration data
FPGA_CONFIG_D1	C2	2.5-V	FPGA configuration data
FPGA_CONFIG_D2	C3	2.5-V	FPGA configuration data
FPGA_CONFIG_D3	D1	2.5-V	FPGA configuration data
FPGA_CONFIG_D4	D2	2.5-V	FPGA configuration data
FPGA_CONFIG_D5	E4	2.5-V	FPGA configuration data
FPGA_CONFIG_D6	D4	2.5-V	FPGA configuration data
FPGA_CONFIG_D7	E5	2.5-V	FPGA configuration data
HSMC_PRSNTN	B8	2.5-V	HSMC port present
JTAG_5M2210_TDI	L6	2.5-V	MAX V JTAG data in
JTAG_5M2210_TDO	M5	2.5-V	MAX V JTAG data out
JTAG_TCK	P3	2.5-V	MAX V JTAG clock
JTAG_TMS	N4	2.5-V	MAX V JTAG TMS

Table 2–4. MAX V CPLD System Controller Device Pin-Out (Part 4 of 5)

Schematic Signal Name	MAX V CPLD Pin Number	I/O Standard	Description
M570_CLOCK	P11	1.5-V	25-MHz clock to on-board USB-Blaster II
M570_PCIE_JTAG_EN	E11	2.5-V	Reserved
MAX5_CLK	T11	1.5-V	MAX V clock
MAX5_DATA	P5	1.5-V	MAX V data
MAX_CONF_DONE	C11	2.5-V	FPGA configuration done LED
MAX_ERROR	A9	2.5-V	FPGA configuration error LED
MAX_LOAD	B12	2.5-V	FPGA configuration active LED
MAX_RESETN	M9	1.5-V	MAX V reset push button
MV_CLK_50	J12	1.8-V	50-MHz clock input
PGM_CONFIG	D9	2.5-V	Loads the flash memory image identified by the PGM LEDs
PGM_LED0	B9	2.5-V	Flash memory PGM select indicator 0
PGM_LED1	C10	2.5-V	Flash memory PGM select indicator 1
PGM_LED2	D12	2.5-V	Flash memory PGM select indicator 2
PGM_SEL	C9	2.5-V	Toggles the PGM_LED[0:2] sequence
SENSE_CS0N	C12	2.5-V	Power monitor chip select
SENSE_SCK	B6	2.5-V	Power monitor SPI clock
SENSE_SDI	B11	2.5-V	Power monitor SPI data in
SENSE_SDO	B10	2.5-V	Power monitor SPI data out
SENSE_SMB_CLK	E7	2.5-V	Temperature monitor SMB clock
SENSE_SMB_DATA	E6	2.5-V	Temperature monitor SMB data
SI53154_SCLK	C8	2.5-V	Si53154 serial clock
SI53154_SDATA	A10	2.5-V	Si53154 serial data
TSENSE_ALERTN_1	D8	2.5-V	FPGA1 temperature monitor alert
TSENSE_ALERTN_2	B5	2.5-V	FPGA2 temperature monitor alert
USB_CFG0	P8	1.5-V	On-board USB Blaster II configuration
USB_CFG1	N6	1.5-V	On-board USB Blaster II configuration
USB_CFG2	M6	1.5-V	On-board USB Blaster II configuration
USB_CFG3	M7	1.5-V	On-board USB Blaster II configuration
USB_CFG4	N8	1.5-V	On-board USB Blaster II configuration
USB_CFG5	N7	1.5-V	On-board USB Blaster II configuration
USB_CFG6	P9	1.5-V	On-board USB Blaster II configuration
USB_CFG7	N11	1.5-V	On-board USB Blaster II configuration
USB_CFG8	T9	1.5-V	On-board USB Blaster II configuration
USB_CFG9	T10	1.5-V	On-board USB Blaster II configuration
USB_CFG10	R9	1.5-V	On-board USB Blaster II configuration
USB_CFG11	T8	1.5-V	On-board USB Blaster II configuration
USB_CFG12	R16	1.5-V	On-board USB Blaster II configuration
USB_CFG13	T13	1.5-V	On-board USB Blaster II configuration

Table 2–4. MAX V CPLD System Controller Device Pin-Out (Part 5 of 5)

Schematic Signal Name	MAX V CPLD Pin Number	I/O Standard	Description
USB_CFG14	T15	1.5-V	On-board USB Blaster II configuration
USB_CLK	H5	2.5-V	On-board USB Blaster II clock

Configuration, Status, and Setup Elements

This section describes the board's configuration, status, and setup elements.

Configuration

This section describes the FPGA, flash memory, and MAX V CPLD System Controller device programming methods that the Stratix V Advanced Systems development board supports.

The Stratix V Advanced Systems development board supports three configuration methods:

- On-Board USB-Blaster II is the default method for configuring the FPGA using the Quartus II Programmer in JTAG mode with the supplied mini-USB cable.
- Parallel flash memory download for configuring the FPGAs using stored images from the flash memory via FPP at either board power-up or by pressing the program configuration push button (S2).
- Serial flash memory download for configuring either FPGA at board power-up via active serial (x4 AS).
- External USB-Blaster for configuring the FPGA using an external USB-Blaster.

FPGA Programming over On-Board USB-Blaster II

The on-board USB-Blaster II is implemented using a mini-USB type-B connector (J6), a USB 2.0 PHY device, and an Altera MAX II CPLD EPM570F100 (U77). This allows for FPGA configuration using a USB cable that connects directly between the USB port on the board and a USB port on a PC running the Quartus II software. The on-board USB-Blaster II masters the JTAG chain.

For more information about the on-board USB-Blaster II, refer to the on-board USB-Blaster II page of the Altera Wiki website.

MAX II CPLD EPM570F100

The MAX II CPLD is dedicated to the on-board USB-Blaster II function. The CPLD connects to the USB 2.0 PHY device on one side and drives the JTAG signals out the other side through the general purpose I/O (GPIO) pins.

Table 2–5 lists the I/O signals present on the MAX II CPLD EPM570F100.

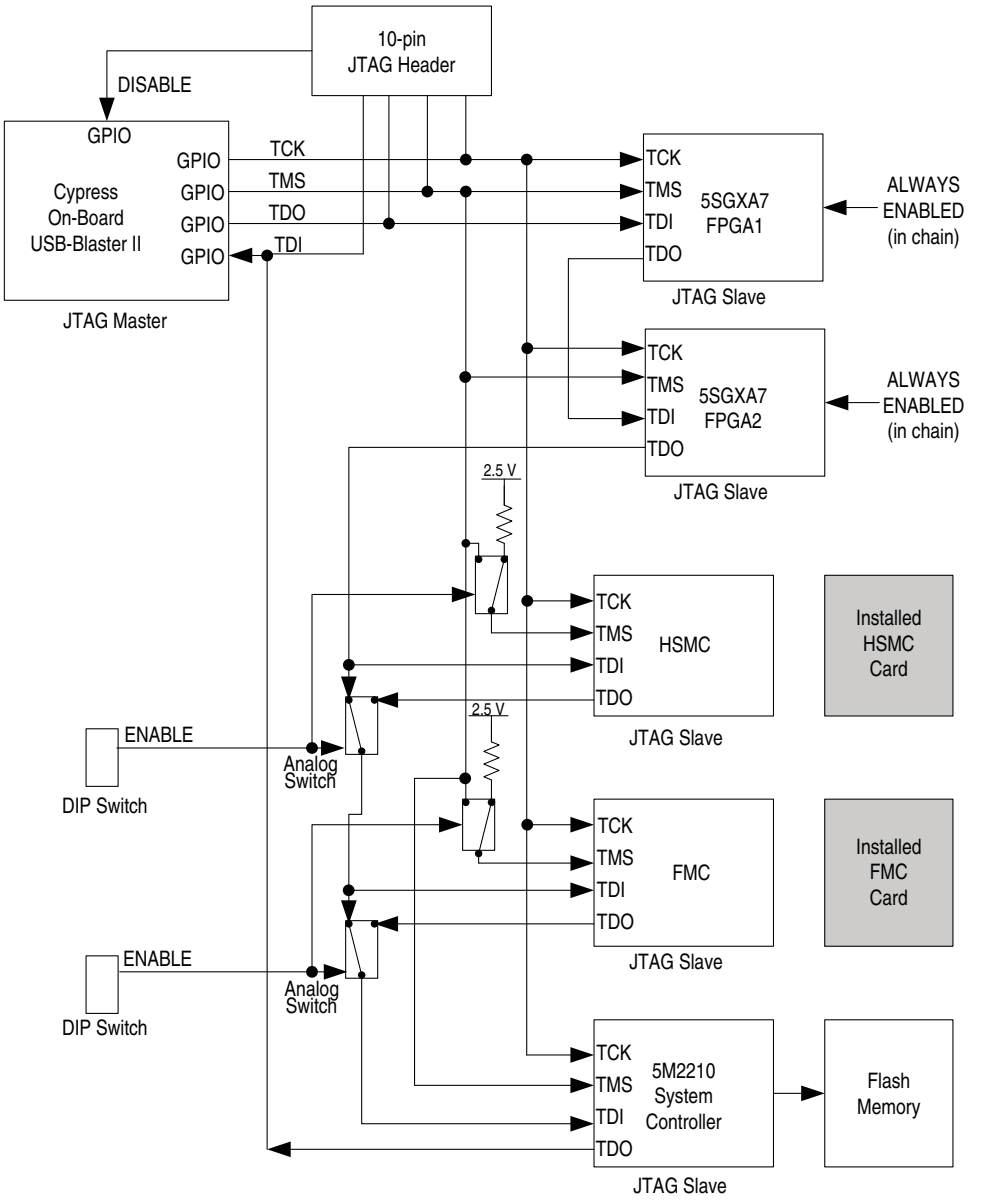
Table 2–5. MAX II CPLD On-Board USB-Blaster II I/O Signals

Schematic Signal Name	Type	Description
SC_RX	1.5-V CMOS output	USB system console receive LED
SC_TX	1.5-V CMOS output	USB system console transmit LED
JTAG_RX	1.5-V CMOS output	USB-Blaster II JTAG receive LED
JTAG_TX	1.5-V CMOS output	USB-Blaster II JTAG transmit LED
C_JTAG_TCK	2.5-V CMOS output	GPIO for on-board JTAG chain clock
C_JTAG_TMS	2.5-V CMOS output	GPIO for on-board JTAG chain mode
C_JTAG_TDI	2.5-V CMOS output	GPIO for on-board JTAG chain data in
C_JTAG_TDO	2.5-V CMOS input	GPIO for on-board JTAG chain data out
USB_CFG(14:0)	1.5-V CMOS input/output	Configuration data between the MAX V System Controller and the on-board USB-Blaster II.
USB_CLK	2.5-V CMOS input	USB System Console clock
USB_OEn	1.5-V CMOS input	USB System Console FPGA output enable
USB_RESETn	1.5-V CMOS input	USB System Console reset
USB_DATA(7:0)	1.5-V CMOS inout (8 bits)	USB System Console FIFO data bus
USB_RDn	1.5-V CMOS input	USB System Console read from FIFO
USB_WRn	1.5-V CMOS input	USB System Console write to FIFO
USB_EMPTY	1.5-V CMOS output	USB System Console FIFO empty
USB_FULL	1.5-V CMOS output	USB System Console FIFO full
USB_ADDR(1:0)	1.5-V CMOS input/output	USB System Console address bus
USB_SCL	1.5-V CMOS input/output	USB System Console configuration clock
USB_SDA	1.5-V CMOS input/output	USB System Console configuration data
FACTORY_REQUEST	1.5-V CMOS input	Send FACTORY command
FACTORY_STATUS	1.5-V CMOS output	FACTORY command status
M570_CLOCK	1.5-V CMOS input	25-MHz input clock for FACTORY command

JTAG Chain

The on-board USB-Blaster II is automatically disabled when you connect an external USB-Blaster to the JTAG chain or when you enable JTAG from the PCI Express edge connector. Figure 2–3 illustrates the JTAG chain.

Figure 2–3. JTAG Chain



Each jumper shown in Figure 2–3 is located in the JTAG DIP switch (SW7) on the back of the board. Both the Stratix V FPGAs and the MAX VSystem Controller are always in the JTAG chain. To connect the HSMC or FMC interface in the chain, their corresponding switch must be in the OFF position.

By default, the on-board USB-Blaster II clocks TCK at 24 MHz. For the on-board USB-Blaster II to function correctly, you must set the Quartus II clock constraint on the altera_reserved_tck input signal to 24 MHz.

System Console USB Interface

The System Console USB interface is a fast parallel interface available on FPGA1. Together with the soft logic supplied by Altera, this interface provides a System Console master for debug access.

The System Console controls the debug master via signals shown in Table 2–6 to give fast access to an Avalon® Memory-Mapped (Avalon-MM) master bus that the Qsys system integration tool generates.

For more information about the System Console, refer to the *Analyzing and Debugging Designs with the System Console* chapter in volume 3 of the *Quartus II Handbook*.

Table 2–6 lists the System Console USB interface pin connections relative to the FPGA.

Table 2–6. System Console USB Interface Pin Connections

Stratix V GX FPGA1 (U29) Pin Number	Schematic Signal Name	Direction	Note
BC8	usb_clk	input	48 MHz
BD34	usb_resetn	input	—
BA15, AJ13, AR16, AH13, BD14, AF17, BC14, AP13	usb_data[7:0]	bidirectional	BA15 (MSB), AP13 (LSB)
AW33	usb_full	output	—
AU35	usb_empty	output	—
AJ29	usb_wrn	input	—
AT33	usb_rdn	input	—
AV34	usb_oen	input	—
AF13, BD10	usb_addr[1:0]	bidirectional	Reserved
BD35	usb_scl	bidirectional	—
BA31	usb_sda	bidirectional	—

CFI Flash Programming

Flash programming is possible using the pre-built PFL design included in the development kit to write configuration data to the CFI flash. The development board implements the Altera PFL megafunction for flash programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device, in this case, the MAX V CPLD. The PFL functions as a utility for writing to a compatible flash device.

This pre-built design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash over the on-board USB-Blaster II interface using the Quartus II software.

Use this method to restore the development board to its factory default settings.

FPGA Programming from CFI Flash Memory

On either board power-up or by pressing the program load push button (S2), the MAX V CPLD System Controller's parallel flash loader configures the FPGA from the flash memory. The system controller uses the Altera Parallel Flash Loader (PFL) megafunction which reads 16-bit data from the flash memory and converts it to fast passive parallel (FPP) format. This 16-bit data is then written to the FPGA's dedicated configuration pins during configuration.

After a board power-up or reset event, the MAX V CPLD (U73) automatically configures the FPGAs in FPP mode with the pre-installed factory **.pof** file. There are three pages reserved for the FPGA configuration data—factory FPGA1 (page 0), factory FPGA2 (page 1), and user design FPGA1 (page 2).

You must set the FPGA1_MSEL[4:0] or FPGA2_MSEL[4:0] DIP switch to FPP x8 mode to configure FPGA1 or FPGA2 via FPP.

For more information about the FPP configuration mode, refer to the *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices* chapter in the *Stratix V Handbook*.

Three green configuration status LEDs, `PGM_LED[2:0]` (D1, D2, D3) indicates the status of the FPP configuration. Table 2–7 lists the configuration status LEDs settings.

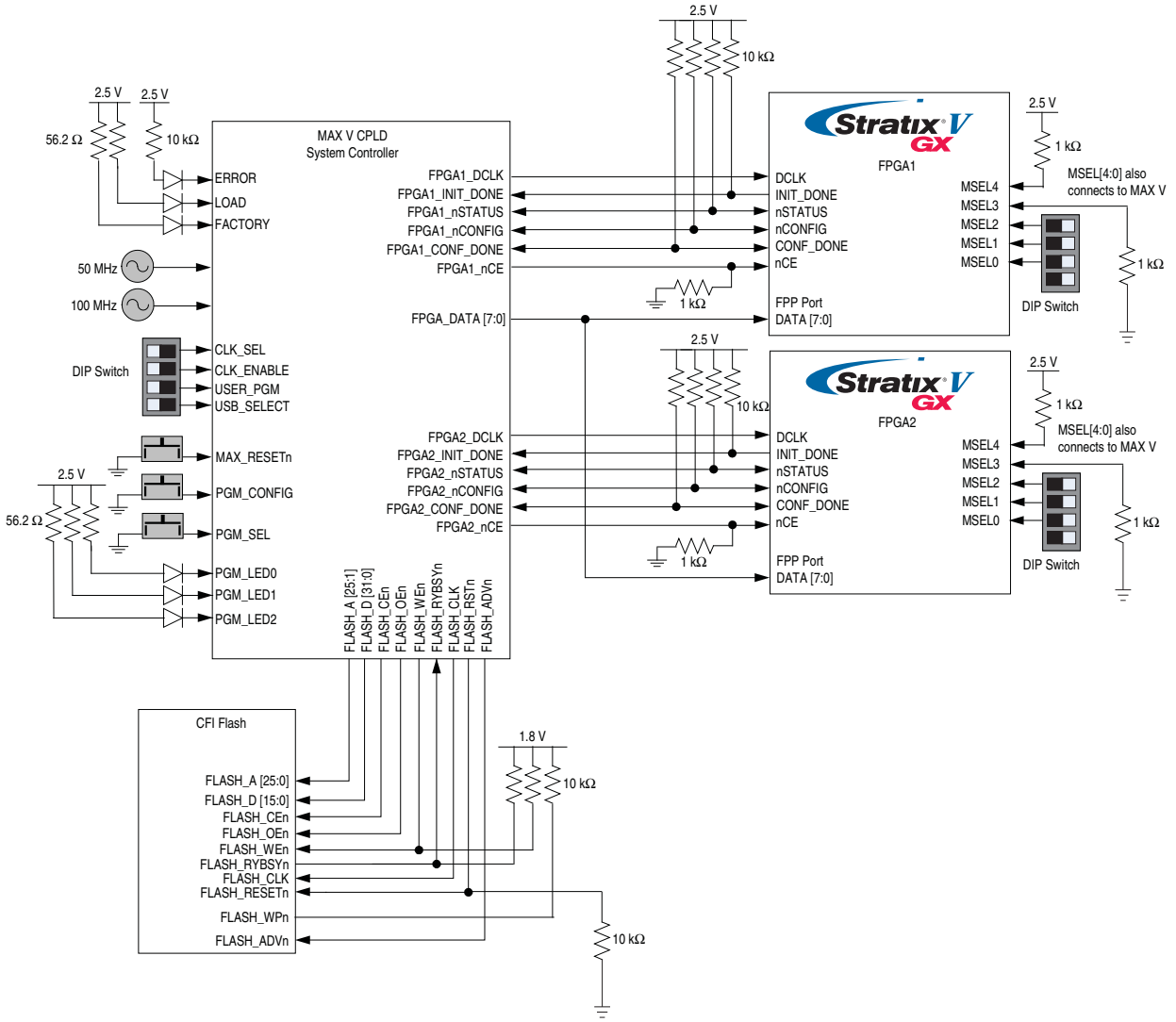
Table 2–7. Configuration LED settings (1)

LED			Design
PGM_LED0	PGM_LED1	PGM_LED2	
✓	—	—	Factory FPGA1
—	✓	—	Factory FPGA2
—	—	✓	User design FPGA1

Note to Table 2–7:
(1) A checkmark (✓) indicates that the LED is ON (logic 0) while a dash (—) indicates that the LED is OFF (logic 1).

Figure 2–4 shows the PFL configuration.

Figure 2–4. PFL Configuration



For more information on the flash memory map storage, refer to the *Stratix V Advanced Systems Development Kit User Guide*.

FPGA Programming from Serial Flash Memory

Each FPGA has an EPCQ (serial flash memory) that connects to it's Active Serial (AS) configuration pins. On board power-up, each FPGA can be configured via AS x4 mode from the EPCQ device. The contents of the EPCQ devices are written using the Altera Serial Flash Loader through the Stratix V GX FPGAdevice.

To write to the EPCQ device or configure the FPGA via AS x4 mode, the respective FPGA must have it's MSEL[4:0] pins set to AS x4 mode.

For more information about the AS configuration mode, refer to the *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices* chapter in the *Stratix V Handbook*.

FPGA Programming over External USB-Blaster

The JTAG programming header provides another method for configuring the FPGA using an external USB-Blaster device with the Quartus II Programmer running on a PC. The external USB-Blaster connects to the board through the JTAG header (J11). When you install the external USB-Blaster into the JTAG header, the on-board USB-Blaster II device is automatically disabled to prevent contention between these two JTAG masters.

For more information on the following topics, refer to the respective documents:

- SFL megafunction, refer to *AN 370: Using the Serial Flash Loader with the Quartus II Software*.
- PFL megafunction, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software.*

Status Elements

The development board includes board-specific status LEDs and switches for enabling and configuring various features on the board. This section describes these status elements.

Status LEDs

Surface mount LEDs indicate various status of the board. A logic 0 is driven on the I/O port to turn on the LED while a logic 1 is driven to turn off the LED.

Table 2–8 lists the LED board references, names, and functional descriptions.

Table 2–8. Board-Specific LEDs (Part 1 of 2)

Board Reference	LED Name	Schematic Signal Name	Description
D27	PWR	—	Blue LED. Illuminates when 5.0-V power is active.
D14	ERROR	MAX_ERROR	Red LED. Illuminates when the MAX V CPLD System Controller fails to configure the FPGA. Driven by the MAX V CPLD System Controller.
D12	LOAD	MAX_LOAD	Green LED. Illuminates when the MAX V CPLD System Controller is actively configuring the FPGA. Driven by the MAX V CPLD System Controller.
D13	CONF_DONE	MAX_CONF_DONEn	Green LED. Illuminates when the FPGA is successfully configured. Driven by the MAX V CPLD System Controller.
D34	FMC_RX	FMC_RX_LED	Green LED. Blinks to indicate FMC receive activity. Driven by FPGA1.
D35	FMC_TX	FMC_TX_LED	Green LED. Blinks to indicate FMC transmit activity. Driven by FPGA1.
D36	FMC_PRSNTn	FMC_PRSNTn	Green LED. Illuminates when the FMC is installed. Driven by the FMC.

Table 2–8. Board-Specific LEDs (Part 2 of 2)

Board Reference	LED Name	Schematic Signal Name	Description
D10	RX	HSMC_RX_LED	Green LED. Blinks to indicate HSMC receive activity. Driven by FPGA2.
D11	TX	HSMC_TX_LED	Green LED. Blinks to indicate HSMC transmit activity. Driven by FPGA2.
D21	PRSNTn	HSMC_PRSNTn	Green LED. Illuminates when the HSMC port has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.
D1, D2, D3	PGM_LED[2:0]	PGM_LED0 PGM_LED1 PGM_LED2	The sequence displayed determines which design is used to configure the FPGAs from flash when you press the PGM_LOAD push button. Refer to Table 2–7 for the push button configuration settings.
D26	OVERTEMP FPGA1	FPGA1_OVERTEMPn	Red LED. Illuminates when a heat sink or fan should be installed. Driven by the MAX1619 thermal sensor FPGA1_OVERTEMPn signal.
D37	OVERTEMP FPGA2	FPGA2_OVERTEMPn	Red LED. Illuminates when a heat sink or fan should be installed. Driven by the MAX1619 thermal sensor FPGA2_OVERTEMPn signal.

Setup Elements

The development board includes several different kinds of setup elements. This section describes the following setup elements:

- Board settings DIP switch
- JTAG control DIP switch
- PCI Express control DIP switch
- MAX V reset push button
- Program load push button
- Program select push button
- CPU reset push buttons

For more information about the DIP switch settings, refer to the *Stratix V Advanced Systems Development Kit User Guide*.

Board Settings DIP Switch

The board settings DIP switch (SW4) controls various features specific to the board and the MAX V CPLD System Controller logic design. Table 2–9 lists the switch controls and descriptions.

Table 2–9. Board Settings DIP Switch Controls

Switch (SW4)	Schematic Signal Name	Description
1	CLK_SEL	ON: SMA input clock select. OFF: Programmable oscillator input clock select (default 100 MHz).
2	CLK_ENABLE	ON: Disable on-board oscillator. OFF: Enable on-board oscillator.
3	EXTRA1	Unused
4	EXTRA0	Unused
5	FPGA2_FPP	ON: Load factory design from flash page 1 to FPGA2 at power up. OFF: No design is configured to FPGA2 using FPP x8.
6	FPGA1_FPP	ON: Load factory design from flash page 0 to FPGA1 at power up. OFF: No design is configured to FPGA1 using FPP x8.

JTAG Control DIP Switch

The JTAG control DIP switch (SW7) provides you an option to either remove or include devices in the active JTAG chain. However, both Stratix V GX FPGA devices are always in the JTAG chain. Table 2–10 shows the switch controls and its descriptions.

Table 2–10. JTAG Control DIP Switch Controls

Switch (SW7)	Schematic Signal Name	Description
1	HSMC_JTAG_EN	ON: Bypass HSMC. OFF: HSMC in-chain.
2	FMC_JTAG_EN	ON: Bypass FMC. OFF: FMC in-chain.
3	—	Unused
4	—	Unused

PCI Express Control DIP Switch

The PCI Express control DIP switch (SW8) can enable or disable different configurations. Table 2–11 shows the switch controls and descriptions.

Table 2–11. PCI Express Control DIP Switch Controls (Part 1 of 2)

Switch (SW8)	Schematic Signal Name	Description
1	PCIE_PRSNT2n_x1	ON: Enable x1 presence detect OFF: Disable x1 presence detect
2	PCIE_PRSNT2n_x4	ON: Enable x4 presence detect OFF: Disable x4 presence detect

Table 2–11. PCI Express Control DIP Switch Controls (Part 2 of 2)

Switch (SW8)	Schematic Signal Name	Description
3	PCIE_PRSNT2n_x8	ON: Enable x8 presence detect OFF: Disable x8 presence detect
4	PCIE_PRSNT2n_x16	ON: Enable x16 presence detect OFF: Disable x16 presence detect

MAX V Reset Push Button

The MAX V reset push button, MAX_RESETn (S3) is an input to the MAX V CPLD System Controller. This push button is the default reset for the CPLD logic.

Program Load Push Button

The program load push button, PGM_CONFIG (S2) is an input to the MAX V CPLD System Controller. The push button forces a reconfiguration of the FPGA from flash memory. The location in the flash memory is based on the settings of the PGM_LED[2:0] which is controlled by the program select push button, PGM_SEL (S1).

Program Select Push Button

The program select push button, PGM_SEL (S1) is an input to the MAX V CPLD System Controller. The push button toggles the PGM_LED[2:0]setting that selects which location in the flash memory is used to configure the FPGA. Refer to Table 2–7 for the configuration settings.

CPU Reset Push Buttons

The CPU reset push buttons, FPGA1_CPU_RESETn (S7) and FPGA2_CPU_RESETn (S11) are inputs to the DEV_CLRn pins of the Stratix V GX FPGA1 and FPGA2 devices respectively, and are open-drain I/O pins from the MAX V CPLD System Controller. These push buttons are the default reset for the FPGA logic. The MAX V System Controller also drives this push button during POR.

You must enable the CPU_RESETn signal within the Quartus II software for this reset function to work. Otherwise, the FPGA1_CPU_RESETn and FPGA2_CPU_RESETn act as regular I/O pins. When you enable the signal and then pull the signal high on the board, these push buttons reset every register within the FPGA with a low signal.

Clock Circuitry

This section describes the board's clock inputs and outputs.

On-Board Oscillators

The development board includes a 50-MHz, 100-MHz, and 125-MHz programmable oscillators. Figure 2–5 shows the default frequencies of all external clocks going to the Stratix V Advanced Systems development board.

Figure 2–5. Stratix V Advanced Systems Development Board External Clock Inputs and Default Frequencies

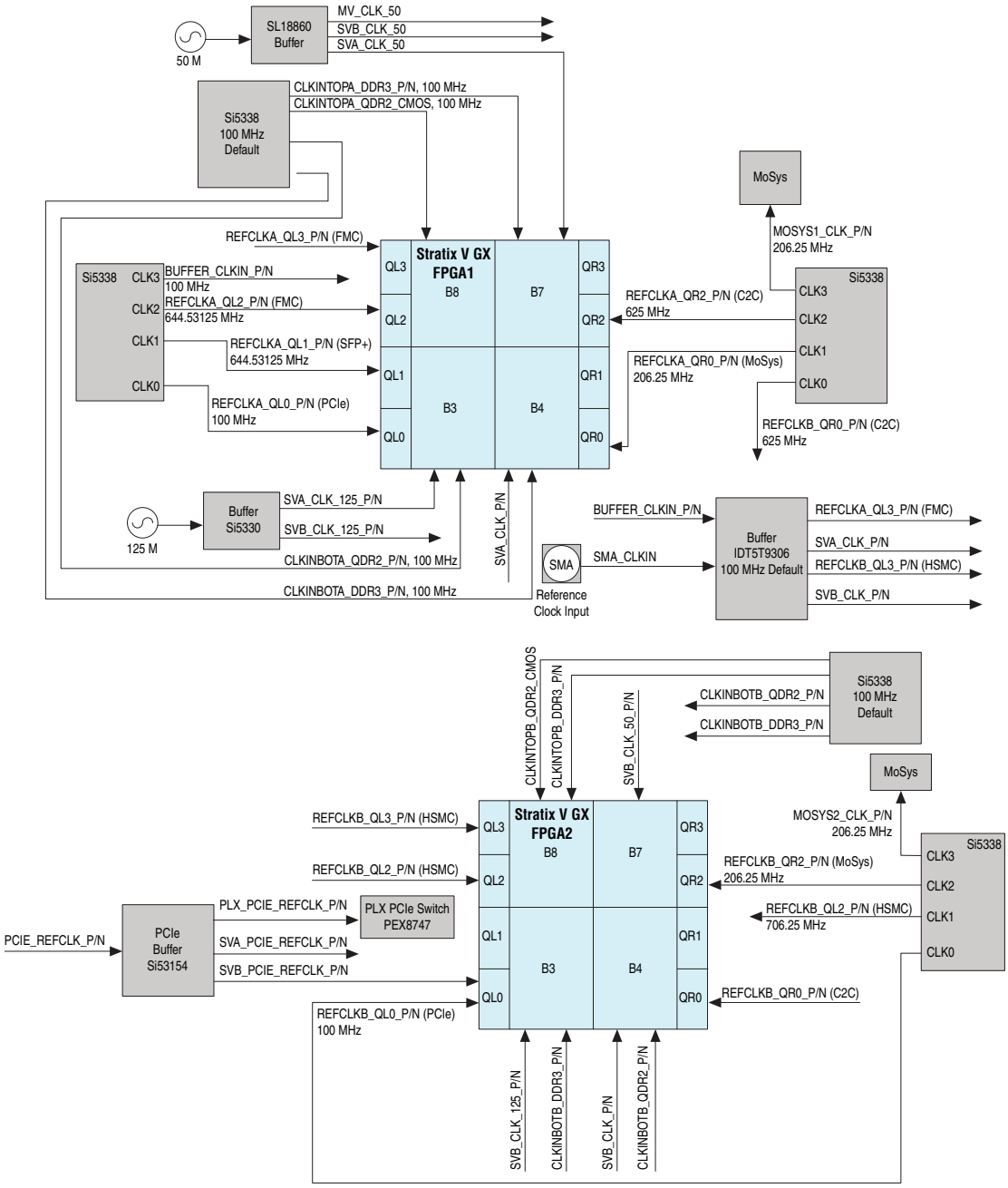


Table 2–12 lists the oscillators, its I/O standard, and voltages required for the development board.

Table 2–12. On-Board Oscillators (Part 1 of 2)

Source	Schematic Signal Name	Frequency	I/O Standard	Stratix V GX FPGA1 Device Pin Number	Stratix V GX FPGA2 Device Pin Number	Application
X2	MV_CLK_50	50.000 MHz	1.8-V CMOS	—	—	MAX V System Controller
	SVB_CLK_50		1.5-V CMOS	—	R25	Nios II
	SVA_CLK_50			R25	—	
X3	CLK_CONFIG	100.000 MHz	2.5-V CMOS	—	—	MAX V Fast FPGA configuration
X1	SVA_CLK_125_P	125.000 MHz	LVDS (fan out buffer)	AW35	—	Nios II
	SVA_CLK_125_N			AY36	—	
	SVB_CLK_125_P			—	AW35	
	SVB_CLK_125_N			—	AY36	
U50	REFCLKA_QL3_P	100.000 MHz (BUFFER_CLKIN_P/N or SMA)	LVDS (fan out buffer)	T38	—	FMC
	REFCLKA_QL3_N			T39	—	
	SVA_CLK_P			AP10	—	General purpose
	SVA_CLK_N			AR10	—	
	REFCLKB_QL3_P			—	V39	HSMC
	REFCLKB_QL3_N			—	V40	
	SVB_CLK_P			—	AP10	General purpose
	SVB_CLK_N			—	AR10	
U91	BUFFER_CLKIN_P	100.000 MHz	LVDS	Buffer Input (U50)		Refer to board reference U50
	BUFFER_CLKIN_N					
	REFCLKA_QL2_P	644.53125 MHz	LVDS	Y38	—	FMC
	REFCLKA_QL2_N			Y39	—	
	REFCLKA_QL1_P	644.53125 MHz	LVDS	AF38	—	FMC
	REFCLKA_QL1_N			AF39	—	
	REFCLKA_QL0_P	100.000 MHz	LVDS	AH39	—	PCI Express
	REFCLKA_QL0_N			AH40	—	
U82	CLKINTOPA_DDR3_P	100.000 MHz (Default)	LVDS	N25	—	DDR3 top edge
	CLKINTOPA_DDR3_N			M25	—	
	CLKINTOPA_QDR2		1.8-V CMOS	B37	—	QDRII+ top edge
	CLKINBOTA_QDR2_P		LVDS	BB18	—	QDRII+ bottom edge
	CLKINBOTA_QDR2_N			BB17	—	
	CLKINBOTA_DDR3_P		LVDS	BB33	—	DDR3 bottom edge
	CLKINBOTA_DDR3_N			BC34	—	

Table 2–12. On-Board Oscillators (Part 2 of 2)

Source	Schematic Signal Name	Frequency	I/O Standard	Stratix V GX FPGA1 Device Pin Number	Stratix V GX FPGA2 Device Pin Number	Application
U100	CLKINTOPB_DDR3_P	100.000 MHz (Default)	LVDS	—	N25	DDR3 top edge
	CLKINTOPB_DDR3_N			—	M25	
	CLKINTOPB_QDR2		1.8-V CMOS	—	B37	QDRII+ top edge
	CLKINBOTB_QDR2_P		LVDS	—	BB18	QDRII+ bottom edge
	CLKINBOTB_QDR2_N			—	BB17	
	CLKINBOTB_DDR3_P		LVDS	—	BB33	DDR3 bottom edge
	CLKINBOTB_DDR3_N			—	BC34	
U53	MOSYS1_REFCLK_P	206.250 MHz	LVDS	—	—	MoSYS MSR576 (U4) reference clock
	MOSYS1_REFCLK_N			—	—	
	REFCLKA_QR2_P	625.000 MHz	LVDS	Y7	—	Chip-to-chip
	REFCLKA_QR2_N			Y6	—	
	REFCLKA_QR0_P	206.250 MHz	LVDS	AK7	—	MoSYS MSR576
	REFCLKA_QR0_N			AK6	—	
	REFCLKB_QR0_P	625.000 MHz	LVDS	—	AK7	Chip-to-chip
	REFCLKB_QR0_N			—	AK6	
U95	MOSYS2_REFCLK_P	206.250 MHz	LVDS	—	—	MoSYS MSR576 (U14) reference clock
	MOSYS2_REFCLK_N			—	—	
	REFCLKB_QR2_P	206.250 MHz	LVDS	—	AB6	MoSYS MSR576
	REFCLKB_QR2_N			—	AB5	
	REFCLKB_QL2_P	706.250 MHz	LVDS	—	AB39	HSMC
	REFCLKB_QL2_N			—	AB40	
	REFCLKB_QL0_P	100.000 MHz	LVDS	—	AH39	Chip-to-chip
	REFCLKB_QL0_N			—	AH40	

Off-Board Clock Input/Output

The development board has input and output clocks which can be driven onto the board. The output clocks can be programmed to different levels and I/O standards according to the FPGA device's specification.

Table 2–13 lists the clock inputs for the development board.

Table 2–13. Off-Board Clock Inputs (Part 1 of 2)

Source	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number	Stratix V GX FPGA2 Device Pin Number	Description
SMA	SMA_CLKIN_P	LVDS	—	—	Input to LVDS fan out buffer (U50)
	SMA_CLKIN_N	LVDS	—	—	

Table 2–13. Off-Board Clock Inputs (Part 2 of 2)

Source	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number	Stratix V GX FPGA2 Device Pin Number	Description
FMC	FMC_CLK_M2C_P[0]	LVDS	J18	—	LVDS clock input from the installed FMC cable or board.
	FMC_CLK_M2C_N[0]	LVDS	H18	—	
	FMC_CLK_M2C_P[1]	LVDS	M9	—	
	FMC_CLK_M2C_N[1]	LVDS	L9	—	
	FMC_LA_RX_CLK_P[0]	LVDS	M8	—	LVDS clock or LVDS general input from the installed FMC cable or board.
	FMC_LA_RX_CLK_N[0]	LVDS	L8	—	
	FMC_LA_RX_CLK_P[1]	LVDS	B8	—	
	FMC_LA_RX_CLK_N[1]	LVDS	A8	—	
	FMC_GBTCLK_M2C_P[0]	LVDS	AB39	—	Transceiver reference clock inputs from the installed FMC cable or board.
	FMC_GBTCLK_M2C_N[0]	LVDS	AB40	—	
	FMC_GBTCLK_M2C_P[1]	LVDS	V39	—	
	FMC_GBTCLK_M2C_N[1]	LVDS	V40	—	
HSMC	HSMC_CLK_IN0	2.5-V	—	BC8	Single-ended input from the installed HSMC cable or board.
	HSMC_CLK_IN_P[1]	LVDS/2.5-V	—	J18	LVDS clock input from the installed HSMC cable or board. Can also support single-ended LVTTL inputs.
	HSMC_CLK_IN_N[1]	LVDS/2.5-V	—	H18	
	HSMC_CLK_IN_P[2]	LVDS/2.5-V	—	M9	
	HSMC_CLK_IN_N[2]	LVDS/2.5-V	—	L9	
PCI Express Edge	PLX_PCIE_REFCLK_P	HCSL	—	—	LVDS input from the PCI Express edge connector.
	PLX_PCIE_REFCLK_N	HCSL	—	—	
	SVA_PCIE_REFCLK_P	HCSL	AK38	—	PCI Express reference clock to fan out buffer (U85).
	SVA_PCIE_REFCLK_N	HCSL	AK39	—	
	SVB_PCIE_REFCLK_P	HCSL	—	AK38	
	SVB_PCIE_REFCLK_N	HCSL	—	AK39	

Table 2–13 lists the clock outputs for the development board.

Table 2–14. Off-Board Clock Outputs

Source	Schematic Signal Name	I/O Standard	Stratix V GX FPGA2 Device Pin Number	Description
HSMC	HSMC_CLK_OUT0	2.5-V CMOS	AR11	FPGA CMOS output (or GPIO).
	HSMC_CLK_OUT_P[1]	LVDS/2.5-V	BC7	LVDS clock output. Can also support single-ended CMOS outputs.
	HSMC_CLK_OUT_N[1]	LVDS/2.5-V	BD7	
	HSMC_CLK_OUT_P[2]	LVDS/2.5-V	B10	
	HSMC_CLK_OUT_N[2]	LVDS/2.5-V	A10	

General User Input/Output

This section describes the user I/O interface to the FPGAs. This section describes the following I/O elements:

- User-defined push buttons
- User-defined DIP switches
- User-defined LEDs

User-Defined Push Buttons

The development board includes three user-defined push buttons for each FPGA device. Board references S4, S5, and S6 are push buttons that allow you to interact with the FPGA1 device while S8, S9, and S10 are to interact with the FPGA2 device. When you press and hold down the push button, the device pin is set to logic 0; when you release the push button, the device pin is set to logic 1. There is no board-specific function for these general user push buttons.

Table 2–15 lists the user-defined push button schematic signal names and their corresponding Stratix V GX FPGA device pin numbers.

Table 2–15. User-Defined Push Button Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number
S4	FPGA1_PB2	1.5-V	BA34
S5	FPGA1_PB1	1.5-V	BA33
S6	FPGA1_PB0	1.5-V	AY33
S8	FPGA2_PB2	1.5-V	U26
S9	FPGA2_PB1	1.5-V	U27
S10	FPGA2_PB0	1.5-V	V26

User-Defined DIP Switches

Board reference SW1 and SW3 are two sets of eight-pin DIP switch, one switch for each FPGA. The switches are user-defined, and are for additional FPGA input control. When the switch is in the CLOSED or ON position, a logic 0 is selected. When the switch is in the OPEN or OFF position, a logic 1 is selected. There is no board-specific function for these switches.

Table 2–16 lists the user-defined DIP switch schematic signal names and their corresponding Stratix V GX FPGA pin numbers.

Table 2–16. User-Defined DIP Switch Schematic Signal Names and Functions (Part 1 of 2)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number
FPGA1 User DIP Switch (SW1)			
1	FPGA1_DIPSW0	1.5-V	V26
2	FPGA1_DIPSW1	1.5-V	V27
3	FPGA1_DIPSW2	1.5-V	AH22

Table 2–16. User-Defined DIP Switch Schematic Signal Names and Functions (Part 2 of 2)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number
4	FPGA1_DIPSW3	1.5-V	AP24
5	FPGA1_DIPSW4	1.5-V	AP25
6	FPGA1_DIPSW5	1.5-V	AH27
7	FPGA1_DIPSW6	1.5-V	AN27
8	FPGA1_DIPSW7	1.5-V	BC29
FPGA2 User DIP Switch (SW3)			
1	FPGA2_DIPSW0	1.5-V	T26
2	FPGA2_DIPSW1	1.5-V	V25
3	FPGA2_DIPSW2	1.5-V	H25
4	FPGA2_DIPSW3	1.5-V	P25
5	FPGA2_DIPSW4	1.5-V	G23
6	FPGA2_DIPSW5	1.5-V	C22
7	FPGA2_DIPSW6	1.5-V	H22
8	FPGA2_DIPSW7	1.5-V	T25

User-Defined LEDs

The development board includes general, FMC, and HSMC user-defined LEDs. This section describes all user-defined LEDs. For information on board specific or status LEDs, refer to"Status Elements" on page 2–18.

General User-Defined LEDs

Board references D6 to D9, D17 to D20, D22 to D25, and D28 to D31 are two sets of eight bi-color user LEDs which allow status and debugging signals to be driven to the LEDs from the designs loaded into the Stratix V GX FPGA device. These LEDs are in red and green, which combines to a total of 16 unique user LEDs. The LEDs illuminate when a logic 0 is driven, and turns off when a logic 1 is driven. There is no board-specific function for these LEDs.

Table 2–17 lists the user-defined LED schematic signal names and their corresponding Stratix V GX FPGA pin numbers.

Table 2–17. User-Defined LED Schematic Signal Names and Functions (Part 1 of 2)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number
FPGA1 User LEDs			
D20.3	FPGA1_LED_G0	1.5-V	H25
D20.4	FPGA1_LED_R0	1.5-V	N22
D19.3	FPGA1_LED_G1	1.5-V	P23
D19.4	FPGA1_LED_R1	1.5-V	P25
D18.3	FPGA1_LED_G2	1.5-V	AH19
D18.4	FPGA1_LED_R2	2.5-V	AR11

Table 2–17. User-Defined LED Schematic Signal Names and Functions (Part 2 of 2)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number
D17.3	FPGA1_LED_G3	2.5-V	AT11
D17.4	FPGA1_LED_R3	1.5-V	AV13
D9.3	FPGA1_LED_G4	1.5-V	G23
D9.4	FPGA1_LED_R4	1.5-V	C22
D8.3	FPGA1_LED_G5	2.5-V	AY9
D8.4	FPGA1_LED_R5	2.5-V	BA9
D7.3	FPGA1_LED_G6	1.5-V	H22
D7.4	FPGA1_LED_R6	1.5-V	N19
D6.3	FPGA1_LED_G7	2.5-V	BB8
D6.4	FPGA1_LED_R7	2.5-V	BD8
FPGA2 User LEDs			
D31.3	FPGA2_LED_G0	1.5-V	N22
D31.4	FPGA2_LED_R0	1.5-V	N19
D30.3	FPGA2_LED_G1	1.5-V	AH19
D30.4	FPGA2_LED_R1	1.5-V	AH22
D29.3	FPGA2_LED_G2	1.5-V	V27
D29.4	FPGA2_LED_R2	1.5-V	P23
D28.3	FPGA2_LED_G3	1.5-V	F16
D28.4	FPGA2_LED_R3	1.5-V	G16
D25.3	FPGA2_LED_G4	1.5-V	AV13
D25.4	FPGA2_LED_R4	1.5-V	AP13
D24.3	FPGA2_LED_G5	1.5-V	AF17
D24.4	FPGA2_LED_R5	1.5-V	AR16
D23.3	FPGA2_LED_G6	1.5-V	AJ13
D23.4	FPGA2_LED_R6	1.5-V	AF13
D22.3	FPGA2_LED_G7	1.5-V	BC14
D22.4	FPGA2_LED_R7	1.5-V	BA15

FMC User-Defined LEDs

The FMC port has three LEDs located nearby. The LEDs illuminate when a daughter card is plugged into the port and also display data flow to and from the connected FMC. The FMC_RX_LED and FMC_TX_LED are driven by the Stratix V GX FPGA1 device. There are no board-specific functions for the FMC LEDs. The FMC_PRSNTn LED illuminates (logic 0) when a card is connected to the FMC port.

Table 2–19 lists the FMC user-defined LED schematic signal names and their corresponding Stratix V GX FPGA1 pin numbers.

Table 2–18. FMC User-Defined LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number
D34	FMC_RX_LED	2.5-V	AN37
D35	FMC_TX_LED	1.5-V	AY34
D36	FMC_PRSNTn	2.5-V	BB9

HSMC User-Defined LEDs

The HSMC port has three LEDs located nearby. The LEDs illuminates when a daughter card is plugged into the port and also displays data flow to and from the connected HSMC. The LEDs are driven by the Stratix V GX FPGA2 device. There are no board-specific functions for the HSMC LEDs.

Table 2–19 lists the HSMC user-defined LED schematic signal names and their corresponding Stratix V GX FPGA2 pin numbers.

Table 2–19. HSMC User-Defined LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA2 Device Pin Number
D10	HSMC_RX_LED	1.5-V	BD14
D11	HSMC_TX_LED	1.5-V	BD10
D21	HSMC_PRSNTn	1.5-V	AH13

Components and Interfaces

This section describes the development board's communication ports and interface cards relative to the Stratix V GX FPGA devices. The development board supports the following communication ports:

- PCI Express
- FMC
- HSMC

PCI Express

The Stratix V Advanced Systems development board is designed to fit entirely into a PC motherboard with a ×16 PCI Express slot that can accommodate a full height long form factor add-in card. This interface uses two Stratix V GX FPGA devices PCI Express hard IP block, saving logic resources for the user logic application. PCI Express x16 is achieved using a PLX PEX8747 PCIe switch to multiplex x16 PCI Express data to x8 PCI Express data to each Stratix V GX FPGA device.

For more information on using the PCI Express hard IP block, refer to the *IP Compiler for PCI Express User Guide*.

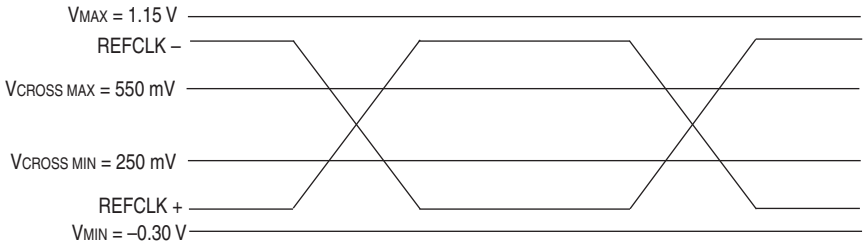
The PCI Express interface supports auto-negotiating channel width from ×1 to ×4 to ×8 to ×16 as well as the connection speed of Gen1 at 2.5 Gbps/lane, Gen2 at 5.0 Gbps/lane, or Gen3 at 8.0 Gbps/lane for a maximum of 128 Gbps full-duplex bandwidth.

The power for the board can be sourced entirely from the PCI Express edge connector when installed into a PC motherboard. Some applications may also require additional power from the PCI Express 2x4 ATX power connector (J10). Although the board can also be powered by a laptop power supply for use on a lab bench, it is not recommended to power from both the PCI Express edge connector and the laptop supplies at the same time. Ideal diode power sharing devices have been designed into this board to prevent damages or back-current from one supply to the other.

The `PCIE_REFCLK_P/N` signal is a 100-MHz differential input that is driven from the PC motherboard to the board through the PCI Express edge connector. This signal connects through a fan out buffer to both Stratix V FPGAs and the PLX switch `REFCLK` input pin pairs. DC coupling on the clock signals is built into the PCI Express clock buffer. This clock is terminated on the motherboard and therefore, no on-board termination is required. This clock can have spread-spectrum properties that change its period between 9.847 ps to 10.203 ps. The I/O standard is High-Speed Current Steering Logic (HCSL).

Figure 2–6 shows the PCI Express reference clock levels.

Figure 2–6. PCI Express Reference Clock Levels



The PCI Express edge connector also has a presence detect feature for the motherboard to determine if a card is installed. A jumper is provided to optionally connect PRSNT1n to any of the four PRSNT2n pins found within the x16 connector definition. This is to address issues on some PC systems that would base the link-width capability on the presence detect pins versus a query operation. Connect any of the four PRSNT2n pins to the PRSNT1n pin using the PCIE_PRSNTn (SW8) DIP switch.

Table 2–20 summarizes the PCI Express pin assignments. The signal names and directions are relative to the Stratix V GX FPGAs.

Table 2–20. PCI Express Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 3)

Board Reference (J13)	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number	Stratix V GX FPGA2 Device Pin Number	Description
A11	PCIE_PERSTn	LVTTL	AU33	AU33	Reset, indicating that the PCI Express main power is stable (3.3 V to 1.8 V translator to Stratix V devices and PEX8747).
A1	PCIE_PRSNT1n	LVTTL	—	—	Presence detect DIP switch
B17	PCIE_PRSNT2n_X1	LVTTL	—	—	Presence detect DIP switch
B31	PCIE_PRSNT2n_X4	LVTTL	—	—	Presence detect DIP switch
B48	PCIE_PRSNT2n_X8	LVTTL	—	—	Presence detect DIP switch
B81	PCIE_PRSNT2n_X16	LVTTL	—	—	Presence detect DIP switch
A14	PCIE_REFCLK_N	HCSL	AK39	AK39	Motherboard reference clock. Fan out buffer to Stratix V devices and PEX8747.
A13	PCIE_REFCLK_P	HCSL	AK38	AK38	Motherboard reference clock. Fan out buffer to Stratix V devices and PEX8747.
B5	PCIE_SMCLK	LVTTL	—	—	SMB clock (optional)
B6	PCIE_SMDAT	LVTTL	—	—	SMB address or data (optional)
B11	PCIE_WAKEn	LVTTL	—	—	Wake signal
U47.A13	PCIE_RX_N0	1.4-V PCML	BB44	—	Receive data bus from PLX switch
U47.A14	PCIE_RX_N1	1.4-V PCML	BA42	—	Receive data bus from PLX switch
U47.A16	PCIE_RX_N2	1.4-V PCML	AW42	—	Receive data bus from PLX switch

Table 2–20. PCI Express Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 3)

Board Reference (J13)	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number	Stratix V GX FPGA2 Device Pin Number	Description
U47.A17	PCIE_RX_N3	1.4-V PCML	AY44	—	Receive data bus from PLX switch
U47.A19	PCIE_RX_N4	1.4-V PCML	AT44	—	Receive data bus from PLX switch
U47.A20	PCIE_RX_N5	1.4-V PCML	AP44	—	Receive data bus from PLX switch
U47.A22	PCIE_RX_N6	1.4-V PCML	AM44	—	Receive data bus from PLX switch
U47.A23	PCIE_RX_N7	1.4-V PCML	AK44	—	Receive data bus from PLX switch
U47.B13	PCIE_RX_P0	1.4-V PCML	BB43	—	Receive data bus from PLX switch
U47.B14	PCIE_RX_P1	1.4-V PCML	BA41	—	Receive data bus from PLX switch
U47.B16	PCIE_RX_P2	1.4-V PCML	AW41	—	Receive data bus from PLX switch
U47.B17	PCIE_RX_P3	1.4-V PCML	AY43	—	Receive data bus from PLX switch
U47.B19	PCIE_RX_P4	1.4-V PCML	AT43	—	Receive data bus from PLX switch
U47.B20	PCIE_RX_P5	1.4-V PCML	AP43	—	Receive data bus from PLX switch
U47.B22	PCIE_RX_P6	1.4-V PCML	AM43	—	Receive data bus from PLX switch
U47.B23	PCIE_RX_P7	1.4-V PCML	AK43	—	Receive data bus from PLX switch
U47.D13	PCIE_TX_N0	1.4-V PCML	AY40	—	Transmit data bus to PLX switch
U47.D14	PCIE_TX_N1	1.4-V PCML	AV40	—	Transmit data bus to PLX switch
U47.D16	PCIE_TX_N2	1.4-V PCML	AT40	—	Transmit data bus to PLX switch
U47.D17	PCIE_TX_N3	1.4-V PCML	AU42	—	Transmit data bus to PLX switch
U47.D19	PCIE_TX_N4	1.4-V PCML	AN42	—	Transmit data bus to PLX switch
U47.D20	PCIE_TX_N5	1.4-V PCML	AL42	—	Transmit data bus to PLX switch
U47.D22	PCIE_TX_N6	1.4-V PCML	AJ42	—	Transmit data bus to PLX switch
U47.D23	PCIE_TX_N7	1.4-V PCML	AG42	—	Transmit data bus to PLX switch
U47.E13	PCIE_TX_P0	1.4-V PCML	AY39	—	Transmit data bus to PLX switch
U47.E14	PCIE_TX_P1	1.4-V PCML	AV39	—	Transmit data bus to PLX switch
U47.E16	PCIE_TX_P2	1.4-V PCML	AT39	—	Transmit data bus to PLX switch
U47.E17	PCIE_TX_P3	1.4-V PCML	AU41	—	Transmit data bus to PLX switch
U47.E19	PCIE_TX_P4	1.4-V PCML	AN41	—	Transmit data bus to PLX switch
U47.E20	PCIE_TX_P5	1.4-V PCML	AL41	—	Transmit data bus to PLX switch
U47.E22	PCIE_TX_P6	1.4-V PCML	AJ41	—	Transmit data bus to PLX switch
U47.E23	PCIE_TX_P7	1.4-V PCML	AG41	—	Transmit data bus to PLX switch
U47.H23	PCIE_RX_N8	1.4-V PCML	—	BB44	Receive data bus from PLX switch
U47.J23	PCIE_RX_N9	1.4-V PCML	—	BA42	Receive data bus from PLX switch
U47.L23	PCIE_RX_N10	1.4-V PCML	—	AW42	Receive data bus from PLX switch
U47.M23	PCIE_RX_N11	1.4-V PCML	—	AY44	Receive data bus from PLX switch
U47.P23	PCIE_RX_N12	1.4-V PCML	—	AT44	Receive data bus from PLX switch
U47.R23	PCIE_RX_N13	1.4-V PCML	—	AP44	Receive data bus from PLX switch
U47.U23	PCIE_RX_N14	1.4-V PCML	—	AM44	Receive data bus from PLX switch
U47.V23	PCIE_RX_N15	1.4-V PCML	—	AK44	Receive data bus from PLX switch
U47.H22	PCIE_RX_P8	1.4-V PCML	—	BB43	Receive data bus from PLX switch

Table 2–20. PCI Express Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 3)

Board Reference (J13)	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number	Stratix V GX FPGA2 Device Pin Number	Description
U47.J22	PCIE_RX_P9	1.4-V PCML	—	BA41	Receive data bus from PLX switch
U47.L22	PCIE_RX_P10	1.4-V PCML	—	AW41	Receive data bus from PLX switch
U47.M22	PCIE_RX_P11	1.4-V PCML	—	AY43	Receive data bus from PLX switch
U47.P22	PCIE_RX_P12	1.4-V PCML	—	AT43	Receive data bus from PLX switch
U47.R22	PCIE_RX_P13	1.4-V PCML	—	AP43	Receive data bus from PLX switch
U47.U22	PCIE_RX_P14	1.4-V PCML	—	AM43	Receive data bus from PLX switch
U47.V22	PCIE_RX_P15	1.4-V PCML	—	AK43	Receive data bus from PLX switch
U47.H20	PCIE_TX_N8	1.4-V PCML	—	AY40	Transmit data bus to PLX switch
U47.J20	PCIE_TX_N9	1.4-V PCML	—	AV40	Transmit data bus to PLX switch
U47.L20	PCIE_TX_N10	1.4-V PCML	—	AT40	Transmit data bus to PLX switch
U47.M20	PCIE_TX_N11	1.4-V PCML	—	AU42	Transmit data bus to PLX switch
U47.P20	PCIE_TX_N12	1.4-V PCML	—	AN42	Transmit data bus to PLX switch
U47.R20	PCIE_TX_N13	1.4-V PCML	—	AL42	Transmit data bus to PLX switch
U47.U20	PCIE_TX_N14	1.4-V PCML	—	AJ42	Transmit data bus to PLX switch
U47.V20	PCIE_TX_N15	1.4-V PCML	—	AG42	Transmit data bus to PLX switch
U47.H19	PCIE_TX_P8	1.4-V PCML	—	AY39	Transmit data bus to PLX switch
U47.J19	PCIE_TX_P9	1.4-V PCML	—	AV39	Transmit data bus to PLX switch
U47.L19	PCIE_TX_P10	1.4-V PCML	—	AT39	Transmit data bus to PLX switch
U47.M19	PCIE_TX_P11	1.4-V PCML	—	AU41	Transmit data bus to PLX switch
U47.P19	PCIE_TX_P12	1.4-V PCML	—	AN41	Transmit data bus to PLX switch
U47.R19	PCIE_TX_P13	1.4-V PCML	—	AL41	Transmit data bus to PLX switch
U47.U19	PCIE_TX_P14	1.4-V PCML	—	AJ41	Transmit data bus to PLX switch
U47.V19	PCIE_TX_P15	1.4-V PCML	—	AG41	Transmit data bus to PLX switch

FMC

The development board supports a FMC front-panel expansion for connectivity via popular standards such as QSFP and SFP+. This low-pin count (LPC) FMC port (J8) connects to the FPGA1 device. This interface provides 10 transceiver channels with 10.3125 Gbps capability. The FMC interface supports both single-ended and differential signaling.

Table 2–22 lists the FMC port pin assignments, signal names, and functions.

Table 2–21. FMC Port Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 5)

Board Reference (J8)	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number	Description
D1	FMC_C2M_PG	3.3-V CMOS	—	Power good output
H4	FMC_CLK_M2C_P0	LVDS	J18	Differential clock input 0
H5	FMC_CLK_M2C_N0		H18	Differential clock input 0

Table 2–21. FMC Port Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 5)

Board Reference (J8)	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number	Description
G2	FMC_CLK_M2C_P1	LVDS	M9	Differential clock input 1
G3	FMC_CLK_M2C_N1		L9	Differential clock input 1
C3	FMC_DP_C2M_N0	1.4-V PCML	W42	Transceiver transmit channel
A23	FMC_DP_C2M_N1	1.4-V PCML	U42	Transceiver transmit channel
A27	FMC_DP_C2M_N2	1.4-V PCML	R42	Transceiver transmit channel
A31	FMC_DP_C2M_N3	1.4-V PCML	N42	Transceiver transmit channel
A35	FMC_DP_C2M_N4	1.4-V PCML	J42	Transceiver transmit channel
A39	FMC_DP_C2M_N5	1.4-V PCML	K40	Transceiver transmit channel
B37	FMC_DP_C2M_N6	1.4-V PCML	H40	Transceiver transmit channel
B33	FMC_DP_C2M_N7	1.4-V PCML	G42	Transceiver transmit channel
B29	FMC_DP_C2M_N8	1.4-V PCML	E42	Transceiver transmit channel
B25	FMC_DP_C2M_N9	1.4-V PCML	D40	Transceiver transmit channel
C2	FMC_DP_C2M_P0	1.4-V PCML	W41	Transceiver transmit channel
A22	FMC_DP_C2M_P1	1.4-V PCML	U41	Transceiver transmit channel
A26	FMC_DP_C2M_P2	1.4-V PCML	R41	Transceiver transmit channel
A30	FMC_DP_C2M_P3	1.4-V PCML	N41	Transceiver transmit channel
A34	FMC_DP_C2M_P4	1.4-V PCML	J41	Transceiver transmit channel
A38	FMC_DP_C2M_P5	1.4-V PCML	K39	Transceiver transmit channel
B36	FMC_DP_C2M_P6	1.4-V PCML	H39	Transceiver transmit channel
B32	FMC_DP_C2M_P7	1.4-V PCML	G41	Transceiver transmit channel
B28	FMC_DP_C2M_P8	1.4-V PCML	E41	Transceiver transmit channel
B24	FMC_DP_C2M_P9	1.4-V PCML	D39	Transceiver transmit channel
C7	FMC_DP_M2C_N0	1.4-V PCML	AB44	Transceiver receive channel
A3	FMC_DP_M2C_N1	1.4-V PCML	Y44	Transceiver receive channel
A7	FMC_DP_M2C_N2	1.4-V PCML	V44	Transceiver receive channel
A11	FMC_DP_M2C_N3	1.4-V PCML	T44	Transceiver receive channel
A15	FMC_DP_M2C_N4	1.4-V PCML	M44	Transceiver receive channel
A19	FMC_DP_M2C_N5	1.4-V PCML	K44	Transceiver receive channel
B17	FMC_DP_M2C_N6	1.4-V PCML	H44	Transceiver receive channel
B13	FMC_DP_M2C_N7	1.4-V PCML	F44	Transceiver receive channel
B9	FMC_DP_M2C_N8	1.4-V PCML	D44	Transceiver receive channel
B5	FMC_DP_M2C_N9	1.4-V PCML	C42	Transceiver receive channel
C6	FMC_DP_M2C_P0	1.4-V PCML	AB43	Transceiver receive channel
A2	FMC_DP_M2C_P1	1.4-V PCML	Y43	Transceiver receive channel
A6	FMC_DP_M2C_P2	1.4-V PCML	V43	Transceiver receive channel
A10	FMC_DP_M2C_P3	1.4-V PCML	T43	Transceiver receive channel
A14	FMC_DP_M2C_P4	1.4-V PCML	M43	Transceiver receive channel
A18	FMC_DP_M2C_P5	1.4-V PCML	K43	Transceiver receive channel

Table 2–21. FMC Port Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 5)

Board Reference (J8)	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number	Description
B16	FMC_DP_M2C_P6	1.4-V PCML	H43	Transceiver receive channel
B12	FMC_DP_M2C_P7	1.4-V PCML	F43	Transceiver receive channel
B8	FMC_DP_M2C_P8	1.4-V PCML	D43	Transceiver receive channel
B4	FMC_DP_M2C_P9	1.4-V PCML	C41	Transceiver receive channel
C34	FMC_GA0	2.5-V CMOS	BD7	Geographic address 0, I^2C channel select
D35	FMC_GA1	2.5-V CMOS	BC7	Geographic address 1, I^2C channel select
D4	FMC_GBTCLK_M2C_P0	LVDS	AB39	Transceiver reference clock
D5	FMC_GBTCLK_M2C_N0		AB40	Transceiver reference clock
B20	FMC_GBTCLK_M2C_P1	LVDS	V39	Transceiver reference clock
B21	FMC_GBTCLK_M2C_N1		V40	Transceiver reference clock
D29	JTAG_TCK	2.5-V CMOS	AL34	JTAG clock
D34	FMC_JTAG_RST	2.5-V CMOS	—	JTAG reset
D30	FMC_JTAG_TDI	2.5-V CMOS	—	JTAG mode select
D31	FMC_JTAG_TDO	2.5-V CMOS	—	JTAG data out
D33	FMC_JTAG_TMS	2.5-V CMOS	—	JTAG data in
G6	FMC_LA_RX_CLK_P0	LVDS (adjustable VCCIO)	M8	LVDS or CMOS clock input
G7	FMC_LA_RX_CLK_N0		L8	LVDS or CMOS clock input
D8	FMC_LA_RX_CLK_P1	LVDS (adjustable VCCIO)	B8	LVDS or CMOS clock input
D9	FMC_LA_RX_CLK_N1		A8	LVDS or CMOS clock input
G10	FMC_LA_RX_N0	LVDS (adjustable VCCIO, 2.5 V default)	H10	LVDS receive or single-ended data bus
C11	FMC_LA_RX_N1		T11	LVDS receive or single-ended data bus
G13	FMC_LA_RX_N2		H8	LVDS receive or single-ended data bus
C15	FMC_LA_RX_N3		V9	LVDS receive or single-ended data bus
G16	FMC_LA_RX_N4		F10	LVDS receive or single-ended data bus
C19	FMC_LA_RX_N5		V11	LVDS receive or single-ended data bus
G19	FMC_LA_RX_N6		F8	LVDS receive or single-ended data bus
C23	FMC_LA_RX_N7		N13	LVDS receive or single-ended data bus
G22	FMC_LA_RX_N8		D9	LVDS receive or single-ended data bus
G25	FMC_LA_RX_N9		C12	LVDS receive or single-ended data bus
G28	FMC_LA_RX_N10		A11	LVDS receive or single-ended data bus
C27	FMC_LA_RX_N11		N14	LVDS receive or single-ended data bus
G31	FMC_LA_RX_N12		F11	LVDS receive or single-ended data bus
G34	FMC_LA_RX_N13		L11	LVDS receive or single-ended data bus
G37	FMC_LA_RX_N14		T9	LVDS receive or single-ended data bus

Table 2–21. FMC Port Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 5)

Board Reference (J8)	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number	Description
G9	FMC_LA_RX_P0	LVDS (adjustable VCCIO, 2.5 V default)	J10	LVDS receive or single-ended data bus
C10	FMC_LA_RX_P1		T12	LVDS receive or single-ended data bus
G12	FMC_LA_RX_P2		H9	LVDS receive or single-ended data bus
C14	FMC_LA_RX_P3		V10	LVDS receive or single-ended data bus
G15	FMC_LA_RX_P4		G10	LVDS receive or single-ended data bus
C18	FMC_LA_RX_P5		V12	LVDS receive or single-ended data bus
G18	FMC_LA_RX_P6		G8	LVDS receive or single-ended data bus
C22	FMC_LA_RX_P7		P13	LVDS receive or single-ended data bus
G21	FMC_LA_RX_P8		E8	LVDS receive or single-ended data bus
G24	FMC_LA_RX_P9		D12	LVDS receive or single-ended data bus
G27	FMC_LA_RX_P10		B11	LVDS receive or single-ended data bus
C26	FMC_LA_RX_P11		P14	LVDS receive or single-ended data bus
G30	FMC_LA_RX_P12		G11	LVDS receive or single-ended data bus
G33	FMC_LA_RX_P13		K11	LVDS receive or single-ended data bus
G36	FMC_LA_RX_P14		U9	LVDS receive or single-ended data bus
H8	FMC_LA_TX_N0	LVDS (adjustable VCCIO, 2.5 V default)	E9	LVDS transmit or single-ended data bus
H11	FMC_LA_TX_N1		C10	LVDS transmit or single-ended data bus
D12	FMC_LA_TX_N2		J12	LVDS transmit or single-ended data bus
H14	FMC_LA_TX_N3		C9	LVDS transmit or single-ended data bus
D15	FMC_LA_TX_N4		J9	LVDS transmit or single-ended data bus
H17	FMC_LA_TX_N5		A7	LVDS transmit or single-ended data bus
D18	FMC_LA_TX_N6		K9	LVDS transmit or single-ended data bus
H20	FMC_LA_TX_N7		R10	LVDS transmit or single-ended data bus
D21	FMC_LA_TX_N8		L12	LVDS transmit or single-ended data bus
H23	FMC_LA_TX_N9		E11	LVDS transmit or single-ended data bus
H26	FMC_LA_TX_N10		H11	LVDS transmit or single-ended data bus
D24	FMC_LA_TX_N11		N8	LVDS transmit or single-ended data bus
H29	FMC_LA_TX_N12		U11	LVDS transmit or single-ended data bus
D27	FMC_LA_TX_N13		M11	LVDS transmit or single-ended data bus
H32	FMC_LA_TX_N14		R12	LVDS transmit or single-ended data bus
H35	FMC_LA_TX_N15		R13	LVDS transmit or single-ended data bus
H38	FMC_LA_TX_N16		T14	LVDS transmit or single-ended data bus

Table 2–21. FMC Port Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 5)

Board Reference (J8)	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number	Description
H7	FMC_LA_TX_P0	LVDS (adjustable VCCIO, 2.5 V default)	F9	LVDS transmit or single-ended data bus
H10	FMC_LA_TX_P1		D11	LVDS transmit or single-ended data bus
D11	FMC_LA_TX_P2		K12	LVDS transmit or single-ended data bus
H13	FMC_LA_TX_P3		D10	LVDS transmit or single-ended data bus
D14	FMC_LA_TX_P4		K8	LVDS transmit or single-ended data bus
H16	FMC_LA_TX_P5		B7	LVDS transmit or single-ended data bus
D17	FMC_LA_TX_P6		K10	LVDS transmit or single-ended data bus
H19	FMC_LA_TX_P7		T10	LVDS transmit or single-ended data bus
D20	FMC_LA_TX_P8		M12	LVDS transmit or single-ended data bus
H22	FMC_LA_TX_P9		E12	LVDS transmit or single-ended data bus
H25	FMC_LA_TX_P10		H12	LVDS transmit or single-ended data bus
D23	FMC_LA_TX_P11		P8	LVDS transmit or single-ended data bus
H28	FMC_LA_TX_P12		U12	LVDS transmit or single-ended data bus
D26	FMC_LA_TX_P13		N11	LVDS transmit or single-ended data bus
H31	FMC_LA_TX_P14		P12	LVDS transmit or single-ended data bus
H34	FMC_LA_TX_P15		T13	LVDS transmit or single-ended data bus
H37	FMC_LA_TX_P16		U14	LVDS transmit or single-ended data bus
F1	FMC_M2C_PG	3.3-V CMOS	—	Power good input
H2	FMC_PRSNTN	2.5-V CMOS	BB9	FMC module present
C30	FMC_SCL	2.5-V CMOS (adjustable VCCIO)	A10	Management serial clock line
C31	FMC_SDA		B10	Management serial data line

HSMC

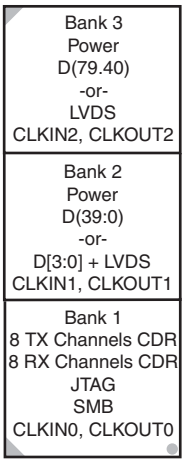
The development board contains a HSMC port that connects to the FPGA2 device. This interface provides 8 channels of 12.5 Gbps-capable transceivers. The HSMC port interface supports both single-ended and differential signaling.

For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, cabling solutions, and mechanical information, refer to the *High Speed Mezzanine Card (HSMC) Specification* manual.

The HSMC connector has a total of 172 pins, including 120 signal pins, 39 power pins, and 13 ground pins. The ground pins are located between two rows of signal and power pins, acting both as a shield and a reference. The HSMC host connector is based on the 0.5 mm-pitch QSH/QTH family of high-speed, board-to-board connectors from Samtec. There are three banks in this connector. Bank 1 has every third pin removed as done in the QSH-DP/QTH-DP series. Bank 2 and bank 3 have all the pins populated as done in the QSH/QTH series.

Figure 2–7 shows the bank arrangement of signals with respect to the Samtec connector's three banks.

Figure 2–7. HSMC Signal and Bank Diagram



The HSMC interface has programmable bi-directional I/O pins that can be used as 2.5-V LVCMOS, which is 3.3-V LVTTL-compatible. You can also use these pins as various differential I/O standards including, but not limited to, LVDS, mini-LVDS, and RSDS with up to 17 full-duplex channels.

☞ As noted in the *High Speed Mezzanine Card (HSMC) Specification* manual, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or generic differential pin-out.

Table 2–22 lists the HSMC port interface pin assignments, signal names, and functions.

Table 2–22. HSMC Port Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference (J1)	Schematic Signal Name	I/O Standard	Stratix V GX FPGA2 Device Pin Number	Description
40	HSMC_CLK_IN0	2.5-V	BC8	Dedicated CMOS clock in
98	HSMC_CLK_IN_N1	LVDS or 2.5-V	H18	LVDS or CMOS clock in 1
158	HSMC_CLK_IN_N2	LVDS or 2.5-V	L9	LVDS or CMOS clock in 2
96	HSMC_CLK_IN_P1	LVDS or 2.5-V	J18	LVDS or CMOS clock in 1 (secondary clock)
156	HSMC_CLK_IN_P2	LVDS or 2.5-V	M9	LVDS or CMOS clock in 2 (primary clock)
39	HSMC_CLK_OUT0	LVDS or 2.5-V	AR11	Dedicated CMOS clock out
97	HSMC_CLK_OUT_N1	LVDS or 2.5-V	BD7	LVDS or CMOS clock out 1
157	HSMC_CLK_OUT_N2	LVDS or 2.5-V	A10	LVDS or CMOS clock out 2
95	HSMC_CLK_OUT_P1	LVDS or 2.5-V	BC7	LVDS or CMOS clock out 1
155	HSMC_CLK_OUT_P2	LVDS or 2.5-V	B10	LVDS or CMOS clock out 2
30	HSMC_RX_P0	1.4-V PCML	AB43	Transceiver receive channel

Table 2–22. HSMC Port Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference (J1)	Schematic Signal Name	I/O Standard	Stratix V GX FPGA2 Device Pin Number	Description
32	HSMC_RX_N0	1.4-V PCML	AB44	Transceiver receive channel
26	HSMC_RX_P1	1.4-V PCML	Y43	Transceiver receive channel
28	HSMC_RX_N1	1.4-V PCML	Y44	Transceiver receive channel
22	HSMC_RX_P2	1.4-V PCML	V43	Transceiver receive channel
24	HSMC_RX_N2	1.4-V PCML	V44	Transceiver receive channel
18	HSMC_RX_P3	1.4-V PCML	T43	Transceiver receive channel
20	HSMC_RX_N3	1.4-V PCML	T44	Transceiver receive channel
14	HSMC_RX_P4	1.4-V PCML	M43	Transceiver receive channel
16	HSMC_RX_N4	1.4-V PCML	M44	Transceiver receive channel
10	HSMC_RX_P5	1.4-V PCML	K43	Transceiver receive channel
12	HSMC_RX_N5	1.4-V PCML	K44	Transceiver receive channel
6	HSMC_RX_P6	1.4-V PCML	H43	Transceiver receive channel
8	HSMC_RX_N6	1.4-V PCML	H44	Transceiver receive channel
2	HSMC_RX_P7	1.4-V PCML	F43	Transceiver receive channel
4	HSMC_RX_N7	1.4-V PCML	F44	Transceiver receive channel
29	HSMC_TX_P0	1.4-V PCML	W41	Transceiver transmit channel
31	HSMC_TX_N0	1.4-V PCML	W42	Transceiver transmit channel
25	HSMC_TX_P1	1.4-V PCML	U41	Transceiver transmit channel
27	HSMC_TX_N1	1.4-V PCML	U42	Transceiver transmit channel
21	HSMC_TX_P2	1.4-V PCML	R41	Transceiver transmit channel
23	HSMC_TX_N2	1.4-V PCML	R42	Transceiver transmit channel
17	HSMC_TX_P3	1.4-V PCML	N41	Transceiver transmit channel
19	HSMC_TX_N3	1.4-V PCML	N42	Transceiver transmit channel
13	HSMC_TX_P4	1.4-V PCML	J41	Transceiver transmit channel
15	HSMC_TX_N4	1.4-V PCML	J42	Transceiver transmit channel
9	HSMC_TX_P5	1.4-V PCML	K39	Transceiver transmit channel
11	HSMC_TX_N5	1.4-V PCML	K40	Transceiver transmit channel
5	HSMC_TX_P6	1.4-V PCML	H39	Transceiver transmit channel
7	HSMC_TX_N6	1.4-V PCML	H40	Transceiver transmit channel
1	HSMC_TX_P7	1.4-V PCML	G41	Transceiver transmit channel
3	HSMC_TX_N7	1.4-V PCML	G42	Transceiver transmit channel
41	HSMC_D0	2.5-V	BB9	Dedicated CMOS I/O bit 0
42	HSMC_D1	2.5-V	AN37	Dedicated CMOS I/O bit 1
43	HSMC_D2	2.5-V	AT11	Dedicated CMOS I/O bit 2
44	HSMC_D3	2.5-V	BD8	Dedicated CMOS I/O bit 3
35	JTAG_TCK	2.5-V	AL34	JTAG clock
38	JTAG_FPGA2_TDO	2.5-V	AL36	JTAG data input
37	HSMC_JTAG_TDO	2.5-V	—	JTAG data output

Table 2–22. HSMC Port Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference (J1)	Schematic Signal Name	I/O Standard	Stratix V GX FPGA2 Device Pin Number	Description
36	HSMC_JTAG_TMS	2.5-V	—	JTAG mode select
160	HSMC_PRSNTn	1.5-V	AH13	HSMC presence detect signal
34	HSMC_SCL	2.5-V	BB36	Management serial clock line
33	HSMC_SDA	2.5-V	BB8	Management serial data line
50	HSMC_RX_D_N0	LVDS or 2.5-V	V11	LVDS RX or CMOS data bus
56	HSMC_RX_D_N1	LVDS or 2.5-V	V9	LVDS RX or CMOS data bus
62	HSMC_RX_D_N2	LVDS or 2.5-V	T9	LVDS RX or CMOS data bus
68	HSMC_RX_D_N3	LVDS or 2.5-V	T11	LVDS RX or CMOS data bus
74	HSMC_RX_D_N4	LVDS or 2.5-V	N14	LVDS RX or CMOS data bus
80	HSMC_RX_D_N5	LVDS or 2.5-V	N13	LVDS RX or CMOS data bus
86	HSMC_RX_D_N6	LVDS or 2.5-V	L11	LVDS RX or CMOS data bus
92	HSMC_RX_D_N7	LVDS or 2.5-V	L8	LVDS RX or CMOS data bus
104	HSMC_RX_D_N8	LVDS or 2.5-V	H10	LVDS RX or CMOS data bus
110	HSMC_RX_D_N9	LVDS or 2.5-V	H8	LVDS RX or CMOS data bus
116	HSMC_RX_D_N10	LVDS or 2.5-V	F11	LVDS RX or CMOS data bus
122	HSMC_RX_D_N11	LVDS or 2.5-V	F8	LVDS RX or CMOS data bus
128	HSMC_RX_D_N12	LVDS or 2.5-V	F10	LVDS RX or CMOS data bus
134	HSMC_RX_D_N13	LVDS or 2.5-V	D9	LVDS RX or CMOS data bus
140	HSMC_RX_D_N14	LVDS or 2.5-V	C12	LVDS RX or CMOS data bus
146	HSMC_RX_D_N15	LVDS or 2.5-V	A11	LVDS RX or CMOS data bus
152	HSMC_RX_D_N16	LVDS or 2.5-V	A8	LVDS RX or CMOS data bus
48	HSMC_RX_D_P0	LVDS or 2.5-V	V12	LVDS RX or CMOS data bus
54	HSMC_RX_D_P1	LVDS or 2.5-V	V10	LVDS RX or CMOS data bus
60	HSMC_RX_D_P2	LVDS or 2.5-V	U9	LVDS RX or CMOS data bus
66	HSMC_RX_D_P3	LVDS or 2.5-V	T12	LVDS RX or CMOS data bus
72	HSMC_RX_D_P4	LVDS or 2.5-V	P14	LVDS RX or CMOS data bus
78	HSMC_RX_D_P5	LVDS or 2.5-V	P13	LVDS RX or CMOS data bus
84	HSMC_RX_D_P6	LVDS or 2.5-V	K11	LVDS RX or CMOS data bus
90	HSMC_RX_D_P7	LVDS or 2.5-V	M8	LVDS RX or CMOS data bus
102	HSMC_RX_D_P8	LVDS or 2.5-V	J10	LVDS RX or CMOS data bus
108	HSMC_RX_D_P9	LVDS or 2.5-V	H9	LVDS RX or CMOS data bus
114	HSMC_RX_D_P10	LVDS or 2.5-V	G11	LVDS RX or CMOS data bus
120	HSMC_RX_D_P11	LVDS or 2.5-V	G8	LVDS RX or CMOS data bus
126	HSMC_RX_D_P12	LVDS or 2.5-V	G10	LVDS RX or CMOS data bus
132	HSMC_RX_D_P13	LVDS or 2.5-V	E8	LVDS RX or CMOS data bus
138	HSMC_RX_D_P14	LVDS or 2.5-V	D12	LVDS RX or CMOS data bus
144	HSMC_RX_D_P15	LVDS or 2.5-V	B11	LVDS RX or CMOS data bus
150	HSMC_RX_D_P16	LVDS or 2.5-V	B8	LVDS RX or CMOS data bus

Table 2–22. HSMC Port Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference (J1)	Schematic Signal Name	I/O Standard	Stratix V GX FPGA2 Device Pin Number	Description
49	HSMC_TX_D_N0	LVDS or 2.5-V	T14	LVDS TX or CMOS data bus
55	HSMC_TX_D_N1	LVDS or 2.5-V	U11	LVDS TX or CMOS data bus
61	HSMC_TX_D_N2	LVDS or 2.5-V	R13	LVDS TX or CMOS data bus
67	HSMC_TX_D_N3	LVDS or 2.5-V	R10	LVDS TX or CMOS data bus
73	HSMC_TX_D_N4	LVDS or 2.5-V	R12	LVDS TX or CMOS data bus
79	HSMC_TX_D_N5	LVDS or 2.5-V	N8	LVDS TX or CMOS data bus
85	HSMC_TX_D_N6	LVDS or 2.5-V	M11	LVDS TX or CMOS data bus
91	HSMC_TX_D_N7	LVDS or 2.5-V	L12	LVDS TX or CMOS data bus
103	HSMC_TX_D_N8	LVDS or 2.5-V	J12	LVDS TX or CMOS data bus
109	HSMC_TX_D_N9	LVDS or 2.5-V	J9	LVDS TX or CMOS data bus
115	HSMC_TX_D_N10	LVDS or 2.5-V	K9	LVDS TX or CMOS data bus
121	HSMC_TX_D_N11	LVDS or 2.5-V	H11	LVDS TX or CMOS data bus
127	HSMC_TX_D_N12	LVDS or 2.5-V	E11	LVDS TX or CMOS data bus
133	HSMC_TX_D_N13	LVDS or 2.5-V	E9	LVDS TX or CMOS data bus
139	HSMC_TX_D_N14	LVDS or 2.5-V	C9	LVDS TX or CMOS data bus
145	HSMC_TX_D_N15	LVDS or 2.5-V	C10	LVDS TX or CMOS data bus
151	HSMC_TX_D_N16	LVDS or 2.5-V	A7	LVDS TX or CMOS data bus
47	HSMC_TX_D_P0	LVDS or 2.5-V	U14	LVDS TX or CMOS data bus
53	HSMC_TX_D_P1	LVDS or 2.5-V	U12	LVDS TX or CMOS data bus
59	HSMC_TX_D_P2	LVDS or 2.5-V	T13	LVDS TX or CMOS data bus
65	HSMC_TX_D_P3	LVDS or 2.5-V	T10	LVDS TX or CMOS data bus
71	HSMC_TX_D_P4	LVDS or 2.5-V	P12	LVDS TX or CMOS data bus
77	HSMC_TX_D_P5	LVDS or 2.5-V	P8	LVDS TX or CMOS data bus
83	HSMC_TX_D_P6	LVDS or 2.5-V	N11	LVDS TX or CMOS data bus
89	HSMC_TX_D_P7	LVDS or 2.5-V	M12	LVDS TX or CMOS data bus
101	HSMC_TX_D_P8	LVDS or 2.5-V	K12	LVDS TX or CMOS data bus
107	HSMC_TX_D_P9	LVDS or 2.5-V	K8	LVDS TX or CMOS data bus
113	HSMC_TX_D_P10	LVDS or 2.5-V	K10	LVDS TX or CMOS data bus
119	HSMC_TX_D_P11	LVDS or 2.5-V	H12	LVDS TX or CMOS data bus
125	HSMC_TX_D_P12	LVDS or 2.5-V	E12	LVDS TX or CMOS data bus
131	HSMC_TX_D_P13	LVDS or 2.5-V	F9	LVDS TX or CMOS data bus
137	HSMC_TX_D_P14	LVDS or 2.5-V	D10	LVDS TX or CMOS data bus
143	HSMC_TX_D_P15	LVDS or 2.5-V	D11	LVDS TX or CMOS data bus
149	HSMC_TX_D_P16	LVDS or 2.5-V	B7	LVDS TX or CMOS data bus

Memory

This section describes the development board memory interface support, signal names, types, and connectivity relative to the Stratix V GX FPGA devices. The board has the following memory interfaces:

- DDR3
- QDRII+
- MoSYS SRAM
- Flash

For more information about the memory interfaces, refer to the External Memory Interface Handbook page of the Altera website.

DDR3

Each FPGA device on the development board supports the following interfaces for very high-speed sequential memory access:

- FPGA1—two 64-bit and two 32-bit interfaces
  - 64-bit data bus consists of four x16 DDR3 SDRAM device
  - 32-bit data bus consists of two x16 DDR3 SDRAM device
- FPGA2—two 64-bit and two 32-bit interfaces
  - 64-bit data bus consists of four x16 DDR3 SDRAM device
  - 32-bit data bus consists of two x16 DDR3 SDRAM device

The DDR3 devices on this board have a target speed of 933 MHz DDR for a total theoretical bandwidth of over 716.5 Gbps. These devices run at a minimum frequency of 300 MHz.

Table 2–23 lists the DDR3 devices pin assignments, signal names, and functions for FPGA1.

Table 2–23. FPGA1 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 7)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number		Description
DDR3A_ / DDR3C_ (x32 bit interface)			DDR3A	DDR3C	
N3	A0	1.5-V SSTL Class I	BC20	G28	Address bus
P7	A1	1.5-V SSTL Class I	AP21	A26	Address bus
P3	A2	1.5-V SSTL Class I	AR22	C27	Address bus
N2	A3	1.5-V SSTL Class I	BA22	T27	Address bus
P8	A4	1.5-V SSTL Class I	AY21	G26	Address bus
P2	A5	1.5-V SSTL Class I	AY22	K28	Address bus
R8	A6	1.5-V SSTL Class I	AV20	H27	Address bus
R2	A7	1.5-V SSTL Class I	AW21	J28	Address bus
T8	A8	1.5-V SSTL Class I	AU22	F26	Address bus

Table 2–23. FPGA1 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 7)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number		Description
R3	A9	1.5-V SSTL Class I	BD22	B26	Address bus
L7	A10	1.5-V SSTL Class I	AU20	A28	Address bus
R7	A11	1.5-V SSTL Class I	BC22	D27	Address bus
N7	A12	1.5-V SSTL Class I	AW20	F28	Address bus
T3	A13	1.5-V SSTL Class I	AT21	E27	Address bus
M2	BA0	1.5-V SSTL Class I	BA21	F29	Bank address bus
N8	BA1	1.5-V SSTL Class I	BD20	P26	Bank address bus
M3	BA2	1.5-V SSTL Class I	AU21	B28	Bank address bus
K3	CASN	1.5-V SSTL Class I	AK20	A29	Column address strobe
K9	CKE	1.5-V SSTL Class I	AT20	H29	Clock enable
K7	CLK_N	Differential 1.5-V SSTL Class I	AW22	H26	Differential output clock
J7	CLK_P	Differential 1.5-V SSTL Class I	AV22	J27	Differential output clock
L2	CSN	1.5-V SSTL Class I	BB21	E29	Chip select
E7	DM0	1.5-V SSTL Class I	BB23	D24	Data write mask
D3	DM1	1.5-V SSTL Class I	AN22	P29	Data write mask
E7	DM2	1.5-V SSTL Class I	AU25	D26	Data write mask
D3	DM3	1.5-V SSTL Class I	AL21	U23	Data write mask
E3	DQ0	1.5-V SSTL Class I	AT24	E23	Data bus
F7	DQ1	1.5-V SSTL Class I	AW23	D23	Data bus
F2	DQ2	1.5-V SSTL Class I	AV23	B25	Data bus
F8	DQ3	1.5-V SSTL Class I	AU23	E24	Data bus
H3	DQ4	1.5-V SSTL Class I	BC23	B23	Data bus
H8	DQ5	1.5-V SSTL Class I	BB24	F23	Data bus
G2	DQ6	1.5-V SSTL Class I	AY24	A23	Data bus
H7	DQ7	1.5-V SSTL Class I	BD23	A25	Data bus
D7	DQ8	1.5-V SSTL Class I	AJ21	P27	Data bus
C3	DQ9	1.5-V SSTL Class I	AM20	M28	Data bus
C8	DQ10	1.5-V SSTL Class I	AJ19	M27	Data bus
C2	DQ11	1.5-V SSTL Class I	AM22	N28	Data bus
A7	DQ12	1.5-V SSTL Class I	AG19	L26	Data bus
A2	DQ13	1.5-V SSTL Class I	AL20	P28	Data bus
B8	DQ14	1.5-V SSTL Class I	AG20	N26	Data bus
A3	DQ15	1.5-V SSTL Class I	AJ20	R27	Data bus
E3	DQ16	1.5-V SSTL Class I	AR25	E26	Data bus
F7	DQ17	1.5-V SSTL Class I	AV25	F24	Data bus
F2	DQ18	1.5-V SSTL Class I	AW24	F25	Data bus
F8	DQ19	1.5-V SSTL Class I	AU24	H24	Data bus

Table 2–23. FPGA1 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 7)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number		Description
H3	DQ20	1.5-V SSTL Class I	BD26	J25	Data bus
H8	DQ21	1.5-V SSTL Class I	AY25	J24	Data bus
G2	DQ22	1.5-V SSTL Class I	BA24	G25	Data bus
H7	DQ23	1.5-V SSTL Class I	BC26	H23	Data bus
D7	DQ24	1.5-V SSTL Class I	AL23	N23	Data bus
C3	DQ25	1.5-V SSTL Class I	AK23	L23	Data bus
C8	DQ26	1.5-V SSTL Class I	AL24	T23	Data bus
C2	DQ27	1.5-V SSTL Class I	AK21	K24	Data bus
A7	DQ28	1.5-V SSTL Class I	AM23	U24	Data bus
A2	DQ29	1.5-V SSTL Class I	AJ22	L24	Data bus
B8	DQ30	1.5-V SSTL Class I	AN23	T24	Data bus
A3	DQ31	1.5-V SSTL Class I	AJ23	M23	Data bus
F3	DQS_P0	Differential 1.5-V SSTL Class I	BC25	C25	Data strobe
G3	DQS_N0	Differential 1.5-V SSTL Class I	BD25	C24	Data strobe
C7	DQS_P1	Differential 1.5-V SSTL Class I	AG21	L27	Data strobe
B7	DQS_N1	Differential 1.5-V SSTL Class I	AH21	K27	Data strobe
F3	DQS_P2	Differential 1.5-V SSTL Class I	BA25	K26	Data strobe
G3	DQS_N2	Differential 1.5-V SSTL Class I	BB26	K25	Data strobe
C7	DQS_P3	Differential 1.5-V SSTL Class I	AR23	R24	Data strobe
B7	DQS_N3	Differential 1.5-V SSTL Class I	AT23	P24	Data strobe
K1	ODT	1.5-V SSTL Class I	AR20	G29	On-die termination enable
J3	RASN	1.5-V SSTL Class I	AR21	D29	Row address strobe
T2	RESETN	1.5-V SSTL Class I	AR24	H28	Reset
L3	WEN	1.5-V SSTL Class I	BB20	C28	Write enable
L8	ZQ01	—	—	—	ZQ impedance calibration
L8	ZQ02	—	—	—	ZQ impedance calibration
DDR3B_ / DDR3D_ (x64 bit interface)			DDR3B	DDR3D	
N3	A0	1.5-V SSTL Class I	AJ32	J19	Address bus
P7	A1	1.5-V SSTL Class I	AM32	E17	Address bus
P3	A2	1.5-V SSTL Class I	AR31	K18	Address bus
N2	A3	1.5-V SSTL Class I	AG33	L18	Address bus
P8	A4	1.5-V SSTL Class I	AE29	D18	Address bus

Table 2–23. FPGA1 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 7)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number		Description
P2	A5	1.5-V SSTL Class I	AE33	M18	Address bus
R8	A6	1.5-V SSTL Class I	AJ33	B17	Address bus
R2	A7	1.5-V SSTL Class I	AF34	B19	Address bus
T8	A8	1.5-V SSTL Class I	AD33	H19	Address bus
R3	A9	1.5-V SSTL Class I	AN31	C18	Address bus
L7	A10	1.5-V SSTL Class I	AR32	N17	Address bus
R7	A11	1.5-V SSTL Class I	AP31	E18	Address bus
N7	A12	1.5-V SSTL Class I	AN33	M17	Address bus
T3	A13	1.5-V SSTL Class I	AM31	A17	Address bus
M2	BA0	1.5-V SSTL Class I	AH33	K17	Bank address bus
N8	BA1	1.5-V SSTL Class I	AK33	L17	Bank address bus
M3	BA2	1.5-V SSTL Class I	AK32	H17	Bank address bus
K3	CASN	1.5-V SSTL Class I	AE30	P17	Column address strobe
K9	CKE	1.5-V SSTL Class I	AG32	H16	Clock enable
K7	CLK_N	Differential 1.5-V SSTL Class I	AE32	P18	Differential output clock
J7	CLK_P	Differential 1.5-V SSTL Class I	AD32	P19	Differential output clock
L2	CSN	1.5-V SSTL Class I	AF32	R19	Chip select
E7	DM0	1.5-V SSTL Class I	BC31	F22	Data write mask
D3	DM1	1.5-V SSTL Class I	AK24	L21	Data write mask
E7	DM2	1.5-V SSTL Class I	AN30	V19	Data write mask
D3	DM3	1.5-V SSTL Class I	AG29	W18	Data write mask
E7	DM4	1.5-V SSTL Class I	AV29	H14	Data write mask
D3	DM5	1.5-V SSTL Class I	AV32	P16	Data write mask
E7	DM6	1.5-V SSTL Class I	AV26	U15	Data write mask
D3	DM7	1.5-V SSTL Class I	BA27	C13	Data write mask
E3	DQ0	1.5-V SSTL Class I	AW30	A20	Data bus
F7	DQ1	1.5-V SSTL Class I	BB30	C21	Data bus
F2	DQ2	1.5-V SSTL Class I	BD31	B20	Data bus
F8	DQ3	1.5-V SSTL Class I	BC32	E20	Data bus
H3	DQ4	1.5-V SSTL Class I	BB32	B22	Data bus
H8	DQ5	1.5-V SSTL Class I	AY31	F21	Data bus
G2	DQ6	1.5-V SSTL Class I	BD32	A22	Data bus
H7	DQ7	1.5-V SSTL Class I	BA30	E21	Data bus
D7	DQ8	1.5-V SSTL Class I	AH24	F20	Data bus
C3	DQ9	1.5-V SSTL Class I	AJ24	J21	Data bus
C8	DQ10	1.5-V SSTL Class I	AH28	G20	Data bus
C2	DQ11	1.5-V SSTL Class I	AK26	J22	Data bus

Table 2–23. FPGA1 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 7)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number		Description
A7	DQ12	1.5-V SSTL Class I	AJ28	K21	Data bus
A2	DQ13	1.5-V SSTL Class I	AL26	K22	Data bus
B8	DQ14	1.5-V SSTL Class I	AH25	K20	Data bus
A3	DQ15	1.5-V SSTL Class I	AJ27	G22	Data bus
E3	DQ16	1.5-V SSTL Class I	AR30	P21	Data bus
F7	DQ17	1.5-V SSTL Class I	AP30	M22	Data bus
F2	DQ18	1.5-V SSTL Class I	AU32	R21	Data bus
F8	DQ19	1.5-V SSTL Class I	AT30	R22	Data bus
H3	DQ20	1.5-V SSTL Class I	AH30	T21	Data bus
H8	DQ21	1.5-V SSTL Class I	AH31	T22	Data bus
G2	DQ22	1.5-V SSTL Class I	AJ30	U20	Data bus
H7	DQ23	1.5-V SSTL Class I	AJ31	U21	Data bus
D7	DQ24	1.5-V SSTL Class I	AG27	N20	Data bus
C3	DQ25	1.5-V SSTL Class I	AG28	U18	Data bus
C8	DQ26	1.5-V SSTL Class I	AG25	M20	Data bus
C2	DQ27	1.5-V SSTL Class I	AG30	V18	Data bus
A7	DQ28	1.5-V SSTL Class I	AF28	L20	Data bus
A2	DQ29	1.5-V SSTL Class I	AK29	T18	Data bus
B8	DQ30	1.5-V SSTL Class I	AG26	K19	Data bus
A3	DQ31	1.5-V SSTL Class I	AF29	P20	Data bus
E3	DQ32	1.5-V SSTL Class I	AL28	G14	Data bus
F7	DQ33	1.5-V SSTL Class I	AU28	F13	Data bus
F2	DQ34	1.5-V SSTL Class I	AU29	H13	Data bus
F8	DQ35	1.5-V SSTL Class I	AM28	G13	Data bus
H3	DQ36	1.5-V SSTL Class I	AP27	K16	Data bus
H8	DQ37	1.5-V SSTL Class I	AK27	K13	Data bus
G2	DQ38	1.5-V SSTL Class I	AV28	J13	Data bus
H7	DQ39	1.5-V SSTL Class I	AL27	J16	Data bus
D7	DQ40	1.5-V SSTL Class I	AR29	M14	Data bus
C3	DQ41	1.5-V SSTL Class I	AU31	N16	Data bus
C8	DQ42	1.5-V SSTL Class I	AM29	L14	Data bus
C2	DQ43	1.5-V SSTL Class I	AW32	T16	Data bus
A7	DQ44	1.5-V SSTL Class I	AP28	M15	Data bus
A2	DQ45	1.5-V SSTL Class I	AV31	T17	Data bus
B8	DQ46	1.5-V SSTL Class I	AN28	J15	Data bus
A3	DQ47	1.5-V SSTL Class I	AU30	R16	Data bus
E3	DQ48	1.5-V SSTL Class I	AN25	P15	Data bus
F7	DQ49	1.5-V SSTL Class I	AU27	V15	Data bus
F2	DQ50	1.5-V SSTL Class I	AM25	V13	Data bus

Table 2–23. FPGA1 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 6 of 7)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number		Description
F8	DQ51	1.5-V SSTL Class I	AW26	T15	Data bus
H3	DQ52	1.5-V SSTL Class I	AL25	W14	Data bus
H8	DQ53	1.5-V SSTL Class I	AR26	Y17	Data bus
G2	DQ54	1.5-V SSTL Class I	AT27	V16	Data bus
H7	DQ55	1.5-V SSTL Class I	AM26	W17	Data bus
D7	DQ56	1.5-V SSTL Class I	BD29	C15	Data bus
C3	DQ57	1.5-V SSTL Class I	BB27	B13	Data bus
C8	DQ58	1.5-V SSTL Class I	BB29	D14	Data bus
C2	DQ59	1.5-V SSTL Class I	AW29	B14	Data bus
A7	DQ60	1.5-V SSTL Class I	AY28	E14	Data bus
A2	DQ61	1.5-V SSTL Class I	AW27	A14	Data bus
B8	DQ62	1.5-V SSTL Class I	BA28	F14	Data bus
A3	DQ63	1.5-V SSTL Class I	AY27	A13	Data bus
F3	DQS_P0	Differential 1.5-V SSTL Class I	AY30	D21	Data strobe
G3	DQS_N0	Differential 1.5-V SSTL Class I	BA29	D20	Data strobe
C7	DQS_P1	Differential 1.5-V SSTL Class I	AJ25	H21	Data strobe
B7	DQS_N1	Differential 1.5-V SSTL Class I	AJ26	H20	Data strobe
F3	DQS_P2	Differential 1.5-V SSTL Class I	AL30	V21	Data strobe
G3	DQS_N2	Differential 1.5-V SSTL Class I	AL31	V20	Data strobe
C7	DQS_P3	Differential 1.5-V SSTL Class I	AE27	T20	Data strobe
B7	DQS_N3	Differential 1.5-V SSTL Class I	AE28	T19	Data strobe
F3	DQS_P4	Differential 1.5-V SSTL Class I	AR27	L15	Data strobe
G3	DQS_N4	Differential 1.5-V SSTL Class I	AR28	K14	Data strobe
C7	DQS_P5	Differential 1.5-V SSTL Class I	AK30	V17	Data strobe
B7	DQS_N5	Differential 1.5-V SSTL Class I	AL29	U17	Data strobe
F3	DQS_P6	Differential 1.5-V SSTL Class I	AT26	Y16	Data strobe
G3	DQS_N6	Differential 1.5-V SSTL Class I	AU26	W16	Data strobe
C7	DQS_P7	Differential 1.5-V SSTL Class I	BC28	E15	Data strobe

Table 2–23. FPGA1 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 7 of 7)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number		Description
B7	DQS_N7	Differential 1.5-V SSTL Class I	BD28	D15	Data strobe
K1	ODT	1.5-V SSTL Class I	AE31	R18	On-die termination enable
J3	RASN	1.5-V SSTL Class I	AF31	G17	Row address strobe
T2	RESETN	1.5-V SSTL Class I	AE34	A19	Reset
L3	WEN	1.5-V SSTL Class I	AP33	F17	Write enable
L8	ZQ01	—	—	—	ZQ impedance calibration
L8	ZQ02	—	—	—	ZQ impedance calibration
L8	ZQ03	—	—	—	ZQ impedance calibration
L8	ZQ04	—	—	—	ZQ impedance calibration

Table 2–23 lists the DDR3 devices pin assignments, signal names, and functions for FPGA2.

Table 2–24. FPGA2 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 6)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA2 Device Pin Number		Description
DDR3E_ / DDR3G_ (x32 bit interface)			DDR3E	DDR3G	
N3	A0	1.5-V SSTL Class I	AW20	G28	Address bus
P7	A1	1.5-V SSTL Class I	AT21	G26	Address bus
P3	A2	1.5-V SSTL Class I	BD20	F26	Address bus
N2	A3	1.5-V SSTL Class I	BB20	D29	Address bus
P8	A4	1.5-V SSTL Class I	AU20	A26	Address bus
P2	A5	1.5-V SSTL Class I	BC20	C27	Address bus
R8	A6	1.5-V SSTL Class I	AU21	C28	Address bus
R2	A7	1.5-V SSTL Class I	BA22	B28	Address bus
T8	A8	1.5-V SSTL Class I	BD22	A28	Address bus
R3	A9	1.5-V SSTL Class I	BB21	E27	Address bus
L7	A10	1.5-V SSTL Class I	AY21	H27	Address bus
R7	A11	1.5-V SSTL Class I	AW21	F28	Address bus
N7	A12	1.5-V SSTL Class I	AV20	H28	Address bus
T3	A13	1.5-V SSTL Class I	BC22	D27	Address bus
M2	BA0	1.5-V SSTL Class I	AU22	F29	Bank address bus
N8	BA1	1.5-V SSTL Class I	AT20	B26	Bank address bus
M3	BA2	1.5-V SSTL Class I	BA21	T27	Bank address bus
K3	CASN	1.5-V SSTL Class I	AR21	K28	Column address strobe
K9	CKE	1.5-V SSTL Class I	AP21	G29	Clock enable
K7	CLK_N	Differential 1.5-V SSTL Class I	AW22	H26	Differential output clock

Table 2–24. FPGA2 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 6)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA2 Device Pin Number		Description
J7	CLK_P	Differential 1.5-V SSTL Class I	AV22	J27	Differential output clock
L2	CSN	1.5-V SSTL Class I	AR22	E29	Chip select
E7	DM0	1.5-V SSTL Class I	BD23	P27	Data write mask
D3	DM1	1.5-V SSTL Class I	AM20	E24	Data write mask
E7	DM2	1.5-V SSTL Class I	AV25	K24	Data write mask
D3	DM3	1.5-V SSTL Class I	AL21	F25	Data write mask
E3	DQ0	1.5-V SSTL Class I	AT24	L26	Data bus
F7	DQ1	1.5-V SSTL Class I	AU23	M27	Data bus
F2	DQ2	1.5-V SSTL Class I	AV23	N26	Data bus
F8	DQ3	1.5-V SSTL Class I	BB23	M28	Data bus
H3	DQ4	1.5-V SSTL Class I	BB24	N28	Data bus
H8	DQ5	1.5-V SSTL Class I	AY24	P29	Data bus
G2	DQ6	1.5-V SSTL Class I	BC23	R27	Data bus
H7	DQ7	1.5-V SSTL Class I	AW23	P28	Data bus
D7	DQ8	1.5-V SSTL Class I	AJ20	B23	Data bus
C3	DQ9	1.5-V SSTL Class I	AJ21	D24	Data bus
C8	DQ10	1.5-V SSTL Class I	AG19	A23	Data bus
C2	DQ11	1.5-V SSTL Class I	AN22	E23	Data bus
A7	DQ12	1.5-V SSTL Class I	AJ19	B25	Data bus
A2	DQ13	1.5-V SSTL Class I	AM22	F23	Data bus
B8	DQ14	1.5-V SSTL Class I	AG20	A25	Data bus
A3	DQ15	1.5-V SSTL Class I	AL20	D23	Data bus
E3	DQ16	1.5-V SSTL Class I	AR25	M23	Data bus
F7	DQ17	1.5-V SSTL Class I	AW24	N23	Data bus
F2	DQ18	1.5-V SSTL Class I	AU24	L24	Data bus
F8	DQ19	1.5-V SSTL Class I	AU25	L23	Data bus
H3	DQ20	1.5-V SSTL Class I	BC26	T24	Data bus
H8	DQ21	1.5-V SSTL Class I	AY25	U24	Data bus
G2	DQ22	1.5-V SSTL Class I	BA24	T23	Data bus
H7	DQ23	1.5-V SSTL Class I	BD26	U23	Data bus
D7	DQ24	1.5-V SSTL Class I	AL24	J25	Data bus
C3	DQ25	1.5-V SSTL Class I	AK23	F24	Data bus
C8	DQ26	1.5-V SSTL Class I	AN23	H24	Data bus
C2	DQ27	1.5-V SSTL Class I	AK21	D26	Data bus
A7	DQ28	1.5-V SSTL Class I	AL23	J24	Data bus
A2	DQ29	1.5-V SSTL Class I	AJ22	E26	Data bus
B8	DQ30	1.5-V SSTL Class I	AM23	H23	Data bus
A3	DQ31	1.5-V SSTL Class I	AJ23	G25	Data bus

Table 2–24. FPGA2 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 6)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA2 Device Pin Number		Description
F3	DQS_P0	Differential 1.5-V SSTL Class I	BC25	L27	Data strobe
G3	DQS_N0	Differential 1.5-V SSTL Class I	BD25	K27	Data strobe
C7	DQS_P1	Differential 1.5-V SSTL Class I	AG21	C25	Data strobe
B7	DQS_N1	Differential 1.5-V SSTL Class I	AH21	C24	Data strobe
F3	DQS_P2	Differential 1.5-V SSTL Class I	BA25	R24	Data strobe
G3	DQS_N2	Differential 1.5-V SSTL Class I	BB26	P24	Data strobe
C7	DQS_P3	Differential 1.5-V SSTL Class I	AR23	K26	Data strobe
B7	DQS_N3	Differential 1.5-V SSTL Class I	AT23	K25	Data strobe
K1	ODT	1.5-V SSTL Class I	AK20	H29	On-die termination enable
J3	RASN	1.5-V SSTL Class I	AR20	J28	Row address strobe
T2	RESETN	1.5-V SSTL Class I	AR24	A29	Reset
L3	WEN	1.5-V SSTL Class I	AY22	P26	Write enable
L8	ZQ01	—	—	—	ZQ impedance calibration
L8	ZQ02	—	—	—	ZQ impedance calibration
DDR3F_ / DDR3H_ (x64 bit interface)			DDR3F	DDR3H	
N3	A0	1.5-V SSTL Class I	AP31	E18	Address bus
P7	A1	1.5-V SSTL Class I	AR31	E17	Address bus
P3	A2	1.5-V SSTL Class I	AM31	H17	Address bus
N2	A3	1.5-V SSTL Class I	AE34	M18	Address bus
P8	A4	1.5-V SSTL Class I	AF32	C18	Address bus
P2	A5	1.5-V SSTL Class I	AD33	P17	Address bus
R8	A6	1.5-V SSTL Class I	AF31	A17	Address bus
R2	A7	1.5-V SSTL Class I	AG32	R18	Address bus
T8	A8	1.5-V SSTL Class I	AE29	A19	Address bus
R3	A9	1.5-V SSTL Class I	AJ33	B17	Address bus
L7	A10	1.5-V SSTL Class I	AN31	H19	Address bus
R7	A11	1.5-V SSTL Class I	AK32	D18	Address bus
N7	A12	1.5-V SSTL Class I	AR32	G17	Address bus
T3	A13	1.5-V SSTL Class I	AJ32	B19	Address bus
M2	BA0	1.5-V SSTL Class I	AE33	M17	Bank address bus
N8	BA1	1.5-V SSTL Class I	AH33	N17	Bank address bus
M3	BA2	1.5-V SSTL Class I	AM32	F17	Bank address bus

Table 2–24. FPGA2 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 6)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA2 Device Pin Number		Description
K3	CASN	1.5-V SSTL Class I	AK33	K17	Column address strobe
K9	CKE	1.5-V SSTL Class I	AE31	K18	Clock enable
K7	CLK_N	Differential 1.5-V SSTL Class I	AE32	P18	Differential output clock
J7	CLK_P	Differential 1.5-V SSTL Class I	AD32	P19	Differential output clock
L2	CSN	1.5-V SSTL Class I	AG33	L17	Chip select
E7	DM0	1.5-V SSTL Class I	BA30	E21	Data write mask
D3	DM1	1.5-V SSTL Class I	AG25	K22	Data write mask
E7	DM2	1.5-V SSTL Class I	AN30	R21	Data write mask
D3	DM3	1.5-V SSTL Class I	AJ28	T18	Data write mask
E7	DM4	1.5-V SSTL Class I	AP27	H13	Data write mask
D3	DM5	1.5-V SSTL Class I	AR29	M15	Data write mask
E7	DM6	1.5-V SSTL Class I	AT27	U15	Data write mask
D3	DM7	1.5-V SSTL Class I	BA28	A14	Data write mask
E3	DQ0	1.5-V SSTL Class I	AY31	E20	Data bus
F7	DQ1	1.5-V SSTL Class I	BC32	B20	Data bus
F2	DQ2	1.5-V SSTL Class I	BB32	F22	Data bus
F8	DQ3	1.5-V SSTL Class I	AW30	F21	Data bus
H3	DQ4	1.5-V SSTL Class I	BD32	A22	Data bus
H8	DQ5	1.5-V SSTL Class I	BD31	A20	Data bus
G2	DQ6	1.5-V SSTL Class I	BB30	B22	Data bus
H7	DQ7	1.5-V SSTL Class I	BC31	C21	Data bus
D7	DQ8	1.5-V SSTL Class I	AF29	G22	Data bus
C3	DQ9	1.5-V SSTL Class I	AF28	J21	Data bus
C8	DQ10	1.5-V SSTL Class I	AG29	F20	Data bus
C2	DQ11	1.5-V SSTL Class I	AG26	K21	Data bus
A7	DQ12	1.5-V SSTL Class I	AG30	J22	Data bus
A2	DQ13	1.5-V SSTL Class I	AG27	L21	Data bus
B8	DQ14	1.5-V SSTL Class I	AK29	G20	Data bus
A3	DQ15	1.5-V SSTL Class I	AG28	K20	Data bus
E3	DQ16	1.5-V SSTL Class I	AT30	R22	Data bus
F7	DQ17	1.5-V SSTL Class I	AR30	P21	Data bus
F2	DQ18	1.5-V SSTL Class I	AP30	T22	Data bus
F8	DQ19	1.5-V SSTL Class I	AU32	M22	Data bus
H3	DQ20	1.5-V SSTL Class I	AJ31	U20	Data bus
H8	DQ21	1.5-V SSTL Class I	AH30	V19	Data bus
G2	DQ22	1.5-V SSTL Class I	AJ30	T21	Data bus
H7	DQ23	1.5-V SSTL Class I	AH31	U21	Data bus

Table 2–24. FPGA2 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 6)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA2 Device Pin Number		Description
D7	DQ24	1.5-V SSTL Class I	AK26	P20	Data bus
C3	DQ25	1.5-V SSTL Class I	AH24	L20	Data bus
C8	DQ26	1.5-V SSTL Class I	AK24	K19	Data bus
C2	DQ27	1.5-V SSTL Class I	AH25	U18	Data bus
A7	DQ28	1.5-V SSTL Class I	AL26	N20	Data bus
A2	DQ29	1.5-V SSTL Class I	AH28	W18	Data bus
B8	DQ30	1.5-V SSTL Class I	AJ24	M20	Data bus
A3	DQ31	1.5-V SSTL Class I	AJ27	V18	Data bus
E3	DQ32	1.5-V SSTL Class I	AV29	K13	Data bus
F7	DQ33	1.5-V SSTL Class I	AM28	G14	Data bus
F2	DQ34	1.5-V SSTL Class I	AV28	J13	Data bus
F8	DQ35	1.5-V SSTL Class I	AL27	H14	Data bus
H3	DQ36	1.5-V SSTL Class I	AU29	F13	Data bus
H8	DQ37	1.5-V SSTL Class I	AK27	K16	Data bus
G2	DQ38	1.5-V SSTL Class I	AU28	G13	Data bus
H7	DQ39	1.5-V SSTL Class I	AL28	J16	Data bus
D7	DQ40	1.5-V SSTL Class I	AW32	P16	Data bus
C3	DQ41	1.5-V SSTL Class I	AU30	N16	Data bus
C8	DQ42	1.5-V SSTL Class I	AV32	R16	Data bus
C2	DQ43	1.5-V SSTL Class I	AP28	J15	Data bus
A7	DQ44	1.5-V SSTL Class I	AM29	T16	Data bus
A2	DQ45	1.5-V SSTL Class I	AN28	L14	Data bus
B8	DQ46	1.5-V SSTL Class I	AU31	T17	Data bus
A3	DQ47	1.5-V SSTL Class I	AV31	M14	Data bus
E3	DQ48	1.5-V SSTL Class I	AN25	P15	Data bus
F7	DQ49	1.5-V SSTL Class I	AU27	W17	Data bus
F2	DQ50	1.5-V SSTL Class I	AM26	T15	Data bus
F8	DQ51	1.5-V SSTL Class I	AW26	V16	Data bus
H3	DQ52	1.5-V SSTL Class I	AV26	W14	Data bus
H8	DQ53	1.5-V SSTL Class I	AM25	V13	Data bus
G2	DQ54	1.5-V SSTL Class I	AL25	V15	Data bus
H7	DQ55	1.5-V SSTL Class I	AR26	Y17	Data bus
D7	DQ56	1.5-V SSTL Class I	AW27	C15	Data bus
C3	DQ57	1.5-V SSTL Class I	BD29	A13	Data bus
C8	DQ58	1.5-V SSTL Class I	AY27	D14	Data bus
C2	DQ59	1.5-V SSTL Class I	AY28	B14	Data bus
A7	DQ60	1.5-V SSTL Class I	BA27	F14	Data bus
A2	DQ61	1.5-V SSTL Class I	AW29	B13	Data bus
B8	DQ62	1.5-V SSTL Class I	BB27	E14	Data bus

Table 2–24. FPGA2 DDR3 Devices Pin Assignments, Schematic Signal Names, and Functions (Part 6 of 6)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA2 Device Pin Number		Description
A3	DQ63	1.5-V SSTL Class I	BB29	C13	Data bus
F3	DQS_P0	Differential 1.5-V SSTL Class I	AY30	D21	Data strobe
G3	DQS_N0	Differential 1.5-V SSTL Class I	BA29	D20	Data strobe
C7	DQS_P1	Differential 1.5-V SSTL Class I	AE27	H21	Data strobe
B7	DQS_N1	Differential 1.5-V SSTL Class I	AE28	H20	Data strobe
F3	DQS_P2	Differential 1.5-V SSTL Class I	AL30	V21	Data strobe
G3	DQS_N2	Differential 1.5-V SSTL Class I	AL31	V20	Data strobe
C7	DQS_P3	Differential 1.5-V SSTL Class I	AJ25	T20	Data strobe
B7	DQS_N3	Differential 1.5-V SSTL Class I	AJ26	T19	Data strobe
F3	DQS_P4	Differential 1.5-V SSTL Class I	AR27	L15	Data strobe
G3	DQS_N4	Differential 1.5-V SSTL Class I	AR28	K14	Data strobe
C7	DQS_P5	Differential 1.5-V SSTL Class I	AK30	V17	Data strobe
B7	DQS_N5	Differential 1.5-V SSTL Class I	AL29	U17	Data strobe
F3	DQS_P6	Differential 1.5-V SSTL Class I	AT26	Y16	Data strobe
G3	DQS_N6	Differential 1.5-V SSTL Class I	AU26	W16	Data strobe
C7	DQS_P7	Differential 1.5-V SSTL Class I	BC28	E15	Data strobe
B7	DQS_N7	Differential 1.5-V SSTL Class I	BD28	D15	Data strobe
K1	ODT	1.5-V SSTL Class I	AF34	L18	On-die termination enable
J3	RASN	1.5-V SSTL Class I	AN33	J19	Row address strobe
T2	RESETN	1.5-V SSTL Class I	AE30	R19	Reset
L3	WEN	1.5-V SSTL Class I	AP33	H16	Write enable
L8	ZQ01	—	—	—	ZQ impedance calibration
L8	ZQ02	—	—	—	ZQ impedance calibration
L8	ZQ03	—	—	—	ZQ impedance calibration
L8	ZQ04	—	—	—	ZQ impedance calibration

QDRII+

Each FPGA device on the development board supports four burst-of-4 QDRII+ SRAM memory devices for very-high-speed, low-latency memory access. The QDRII+ has a x18 interface, providing device addressing for up to 72 Mb. Although the additional address bit is available for future migration, the current board is populated with 36 Mb devices.

The QDRII+ has separate read and write data ports with DDR signaling at up to 550 MHz. A maximum theoretical bandwidth of over 158.4 Gbps for reading and 158.4 Gbps for writing is possible using eight interfaces (four interfaces per FPGA). The pinout supports migration to extreme QDRII+ with a 667-MHz interface.

Table 2–25 lists the QDRII+ pin assignments, signal names, and functions for FPGA1.

Table 2–25. FPGA1 QDRII+ Pin Assignments, Signal Names and Functions (Part 1 of 3)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number				Description
			QDR2A	QDR2B	QDR2C	QDR2D	
R9	A0	1.5-V HSTL Class I	BD19	AV11	B31	V34	Address bus
R8	A1	1.5-V HSTL Class I	BD17	AT12	C31	U35	Address bus
B4	A2	1.5-V HSTL Class I	AR18	AU9	R30	M36	Address bus
B8	A3	1.5-V HSTL Class I	AV16	AU11	E33	U32	Address bus
C5	A4	1.5-V HSTL Class I	AT18	AV10	M31	M39	Address bus
C7	A5	1.5-V HSTL Class I	AU17	AU10	J30	M37	Address bus
N5	A6	1.5-V HSTL Class I	AY19	AL11	C36	J36	Address bus
N6	A7	1.5-V HSTL Class I	BA18	AM13	B35	H36	Address bus
N7	A8	1.5-V HSTL Class I	BA16	AR13	B34	L35	Address bus
P4	A9	1.5-V HSTL Class I	AU16	AK12	D36	M33	Address bus
P5	A10	1.5-V HSTL Class I	AY18	AJ11	C34	K35	Address bus
P7	A11	1.5-V HSTL Class I	BA19	AN12	A35	K36	Address bus
P8	A12	1.5-V HSTL Class I	BC19	AR12	B32	K37	Address bus
R3	A13	1.5-V HSTL Class I	AN17	AJ12	T33	N31	Address bus
R4	A14	1.5-V HSTL Class I	AT17	AH12	T32	P33	Address bus
R5	A15	1.5-V HSTL Class I	AY16	AG12	C33	K34	Address bus
R7	A16	1.5-V HSTL Class I	BC17	AL12	A34	H37	Address bus
A9	A17	1.5-V HSTL Class I	AW17	AG10	D33	V33	Address bus
A3	A18	1.5-V HSTL Class I	AP16	AG11	P32	L36	Address bus
A10	A19	1.5-V HSTL Class I	AW16	AG9	D35	T35	Address bus (Unused)
B7	BWSN0	1.5-V HSTL Class I	AJ18	AF11	V30	K32	Write byte write select 0
A5	BWSN1	1.5-V HSTL Class I	AH18	AD14	W29	K31	Write byte write select 1
A1	CQ_N	1.5-V HSTL Class I	AG16	AP15	T30	R36	Echo clock
A11	CQ_P	1.5-V HSTL Class I	AY15	AU12	K30	J37	Echo clock
P10	D0	1.5-V HSTL Class I	AW19	BB11	B29	L32	Write data bus
N11	D1	1.5-V HSTL Class I	AV19	BC10	C30	M34	Write data bus
M11	D2	1.5-V HSTL Class I	AU19	AW11	A31	P34	Write data bus

Table 2–25. FPGA1 QDRII+ Pin Assignments, Signal Names and Functions (Part 2 of 3)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number				Description
			QDR2A	QDR2B	QDR2C	QDR2D	
K10	D3	1.5-V HSTL Class I	AU18	AE13	D30	L33	Write data bus
J11	D4	1.5-V HSTL Class I	AR19	AF10	A32	V35	Write data bus
G11	D5	1.5-V HSTL Class I	AP19	AE12	E30	R34	Write data bus
E10	D6	1.5-V HSTL Class I	AM17	AE9	D32	R33	Write data bus
D11	D7	1.5-V HSTL Class I	AM19	AE10	E32	W34	Write data bus
C11	D8	1.5-V HSTL Class I	AL19	AE11	F31	T34	Write data bus
B3	D9	1.5-V HSTL Class I	AG17	AG13	Y28	J34	Write data bus
C3	D10	1.5-V HSTL Class I	AG18	AE14	Y29	J33	Write data bus
D2	D11	1.5-V HSTL Class I	AJ17	AW10	Y30	H35	Write data bus
F3	D12	1.5-V HSTL Class I	AK17	AF14	Y27	J31	Write data bus
G2	D13	1.5-V HSTL Class I	AK18	AY10	V29	G35	Write data bus
J3	D14	1.5-V HSTL Class I	AL17	BA10	W28	G34	Write data bus
L3	D15	1.5-V HSTL Class I	AL18	AY12	U29	F35	Write data bus
M3	D16	1.5-V HSTL Class I	AN19	BA12	V28	F34	Write data bus
N2	D17	1.5-V HSTL Class I	AN20	BB12	G31	E35	Write data bus
H1	DOFFN	1.5-V HSTL Class I	AP18	AP12	K29	A37	PLL disable
A6	K_N	Differential 1.5-V HSTL Class I	AJ16	BD11	R28	H33	Write clock
B6	K_P	Differential 1.5-V HSTL Class I	AJ15	BC11	T28	H34	Write clock
R6	ODT	—	—	—	—	—	On-die termination, resistor grounded
P11	Q0	1.5-V HSTL Class I	BD16	AR15	N29	P36	Read data bus
M10	Q1	1.5-V HSTL Class I	BD13	AU14	P30	N37	Read data bus
L11	Q2	1.5-V HSTL Class I	BC16	AM16	L29	P37	Read data bus
K11	Q3	1.5-V HSTL Class I	BC13	AM14	M30	P38	Read data bus
J10	Q4	1.5-V HSTL Class I	BB15	AU13	L30	N38	Read data bus
F11	Q5	1.5-V HSTL Class I	BB14	AL16	H31	P39	Read data bus
E11	Q6	1.5-V HSTL Class I	BA13	AL15	F32	U36	Read data bus
C10	Q7	1.5-V HSTL Class I	AK15	AL14	G32	T36	Read data bus
B11	Q8	1.5-V HSTL Class I	AY13	AK14	H32	V36	Read data bus
B2	Q9	1.5-V HSTL Class I	AE16	AR14	V31	W35	Read data bus
D3	Q10	1.5-V HSTL Class I	AE15	AN15	W31	G37	Read data bus
E3	Q11	1.5-V HSTL Class I	AE18	AN14	W32	F36	Read data bus
F2	Q12	1.5-V HSTL Class I	AE17	AT15	Y32	D37	Read data bus
G3	Q13	1.5-V HSTL Class I	AF16	AT14	T31	B39	Read data bus
K3	Q14	1.5-V HSTL Class I	AG14	AU15	U30	B38	Read data bus
L2	Q15	1.5-V HSTL Class I	AG15	AV14	R31	C37	Read data bus
N3	Q16	1.5-V HSTL Class I	AJ14	AW13	P31	A38	Read data bus

Table 2–25. FPGA1 QDRII+ Pin Assignments, Signal Names and Functions (Part 3 of 3)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA1 Device Pin Number				Description
			QDR2A	QDR2B	QDR2C	QDR2D	
P3	Q17	1.5-V HSTL Class I	AH15	AW14	T29	E36	Read data bus
P6	QVLD	—	—	—	—	—	Read data valid (Unused)
A8	RPSN	1.5-V HSTL Class I	AV17	AH10	H30	U33	Read port select
A4	WPSN	1.5-V HSTL Class I	AR17	AJ10	N32	M38	Write port select

Table 2–25 lists the QDRII+ pin assignments, signal names, and functions for FPGA2.

Table 2–26. FPGA2 QDRII+ Pin Assignments, Signal Names and Functions (Part 1 of 3)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number				Description
			QDR2E	QDR2F	QDR2G	QDR2H	
R9	A0	1.5-V HSTL Class I	BD19	AG12	J30	V34	Address bus
R8	A1	1.5-V HSTL Class I	BC19	AG11	M31	U35	Address bus
B4	A2	1.5-V HSTL Class I	AR17	AK12	A35	K34	Address bus
B8	A3	1.5-V HSTL Class I	AU16	AH10	C36	J36	Address bus
C5	A4	1.5-V HSTL Class I	AR18	AJ12	B35	K35	Address bus
C7	A5	1.5-V HSTL Class I	AT17	AJ11	B31	L36	Address bus
N5	A6	1.5-V HSTL Class I	AY16	AU10	D36	M36	Address bus
N6	A7	1.5-V HSTL Class I	BA16	AU9	C31	K37	Address bus
N7	A8	1.5-V HSTL Class I	BA18	AN12	C33	M38	Address bus
P4	A9	1.5-V HSTL Class I	AW16	AU11	P32	M37	Address bus
P5	A10	1.5-V HSTL Class I	AY18	AV10	C34	M33	Address bus
P7	A11	1.5-V HSTL Class I	BC17	AM13	D33	M39	Address bus
P8	A12	1.5-V HSTL Class I	BA19	AH12	E33	T35	Address bus
R3	A13	1.5-V HSTL Class I	AV17	AR13	T33	U32	Address bus
R4	A14	1.5-V HSTL Class I	AW17	AT12	T32	P33	Address bus
R5	A15	1.5-V HSTL Class I	AY19	AV11	N32	K36	Address bus
R7	A16	1.5-V HSTL Class I	BD17	AR12	H30	U33	Address bus
A9	A17	1.5-V HSTL Class I	AU17	AG9	D35	H36	Address bus
A3	A18	1.5-V HSTL Class I	AN17	AL12	R30	L35	Address bus
A10	A19	1.5-V HSTL Class I	AV16	AG10	B34	H37	Address bus (Unused)
B7	BWSN0	1.5-V HSTL Class I	AK17	AE13	Y27	G34	Write byte write select 0
A5	BWSN1	1.5-V HSTL Class I	AJ17	AD14	W28	F34	Write byte write select 1
A1	CQ_N	1.5-V HSTL Class I	AG16	AP15	T30	R36	Echo clock
A11	CQ_P	1.5-V HSTL Class I	AY15	AU12	K30	J37	Echo clock
P10	D0	1.5-V HSTL Class I	AV19	AW11	A32	V35	Write data bus
N11	D1	1.5-V HSTL Class I	AW19	AW10	F31	W34	Write data bus
M11	D2	1.5-V HSTL Class I	AU19	AE14	E32	T34	Write data bus
K10	D3	1.5-V HSTL Class I	AU18	AF11	D32	L33	Write data bus

Table 2–26. FPGA2 QDRII+ Pin Assignments, Signal Names and Functions (Part 2 of 3)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number				Description
			QDR2E	QDR2F	QDR2G	QDR2H	
J11	D4	1.5-V HSTL Class I	AR19	AF10	E30	R34	Write data bus
G11	D5	1.5-V HSTL Class I	AP19	AE9	D30	R33	Write data bus
E10	D6	1.5-V HSTL Class I	AM19	AE12	A31	L32	Write data bus
D11	D7	1.5-V HSTL Class I	AN20	AE10	B29	P34	Write data bus
C11	D8	1.5-V HSTL Class I	AN19	AE11	C30	M34	Write data bus
B3	D9	1.5-V HSTL Class I	AG18	AF14	V30	K32	Write data bus
C3	D10	1.5-V HSTL Class I	AH18	AG13	W29	J33	Write data bus
D2	D11	1.5-V HSTL Class I	AG17	AY10	Y30	J31	Write data bus
F3	D12	1.5-V HSTL Class I	AJ18	BA10	V29	E35	Write data bus
G2	D13	1.5-V HSTL Class I	AK18	AY12	Y29	K31	Write data bus
J3	D14	1.5-V HSTL Class I	AL17	BC10	U29	F35	Write data bus
L3	D15	1.5-V HSTL Class I	AL18	BB11	Y28	J34	Write data bus
M3	D16	1.5-V HSTL Class I	AL19	BA12	V28	G35	Write data bus
N2	D17	1.5-V HSTL Class I	AM17	BB12	G31	H35	Write data bus
H1	DOFFN	1.5-V HSTL Class I	AP18	AP12	K29	A37	PLL disable
A6	K_N	Differential 1.5-V HSTL Class I	AJ16	BD11	R28	H33	Write clock
B6	K_P	Differential 1.5-V HSTL Class I	AJ15	BC11	T28	H34	Write clock
R6	ODT	—	—	—	—	—	On-die termination, resistor grounded
P11	Q0	1.5-V HSTL Class I	AY13	AK14	N29	W35	Read data bus
M10	Q1	1.5-V HSTL Class I	BD16	AL14	P30	T36	Read data bus
L11	Q2	1.5-V HSTL Class I	BC16	AL15	G32	V36	Read data bus
K11	Q3	1.5-V HSTL Class I	BB15	AL16	H31	U36	Read data bus
J10	Q4	1.5-V HSTL Class I	BD13	AM14	H32	P37	Read data bus
F11	Q5	1.5-V HSTL Class I	BC13	AN14	L30	P39	Read data bus
E11	Q6	1.5-V HSTL Class I	BB14	AN15	L29	P38	Read data bus
C10	Q7	1.5-V HSTL Class I	BA13	AR14	F32	P36	Read data bus
B11	Q8	1.5-V HSTL Class I	AE18	AM16	M30	N38	Read data bus
B2	Q9	1.5-V HSTL Class I	AE15	AR15	T31	N37	Read data bus
D3	Q10	1.5-V HSTL Class I	AE16	AU13	R31	F36	Read data bus
E3	Q11	1.5-V HSTL Class I	AG14	AT14	P31	G37	Read data bus
F2	Q12	1.5-V HSTL Class I	AG15	AU14	U30	E36	Read data bus
G3	Q13	1.5-V HSTL Class I	AJ14	AW13	T29	D37	Read data bus
K3	Q14	1.5-V HSTL Class I	AH15	AV14	V31	B38	Read data bus
L2	Q15	1.5-V HSTL Class I	AK15	AW14	W32	C37	Read data bus
N3	Q16	1.5-V HSTL Class I	AF16	AT15	W31	A38	Read data bus
P3	Q17	1.5-V HSTL Class I	AE17	AU15	Y32	B39	Read data bus

Table 2–26. FPGA2 QDRII+ Pin Assignments, Signal Names and Functions (Part 3 of 3)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number				Description
			QDR2E	QDR2F	QDR2G	QDR2H	
P6	QVLD	—	—	—	—	—	Read data valid (Unused)
A8	RPSN	1.5-V HSTL Class I	AT18	AJ10	B32	V33	Read port select
A4	WPSN	1.5-V HSTL Class I	AP16	AL11	A34	N31	Write port select

MoSys MSR576

Each FPGA on the development board supports a 576-Mb MoSys MSR576 Bandwidth Engine SRAM interface for very-high-speed sequential memory access. The 16-bit transceiver based interface can run up to 10.3125 G per channel, which encapsulates four SRAM memory interfaces internally, each with a 2Mx72 configuration. Each interface supports up to 18.6 GB/s read memory bandwidth.

Table 2–27 lists the MoSys MSR576 interface pin assignments, signal names, and functions relative to the Stratix V GX FPGAs.

Table 2–27. MoSys MSR576 Interface Pin Assignments, Signal Names and Functions (Part 1 of 5)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number	Description
FPGA1 MoSys (U4)				
G20	MOSYS1_AMON_0	1.5-V CMOS	—	Analog monitor
B1	MOSYS1_AMON_1	1.5-V CMOS	—	Analog monitor
P22	MOSYS1_CLKDIVIDE	1.5-V CMOS	B16	REFCLK divider enable
A21	MOSYS1_CMDARX_N0	1.4-V PCML	AY5	Transceiver output
C20	MOSYS1_CMDARX_N1	1.4-V PCML	AV5	Transceiver output
A19	MOSYS1_CMDARX_N2	1.4-V PCML	AU3	Transceiver output
C18	MOSYS1_CMDARX_N3	1.4-V PCML	AT5	Transceiver output
A17	MOSYS1_CMDARX_N4	1.4-V PCML	AR3	Transceiver output
C16	MOSYS1_CMDARX_N5	1.4-V PCML	AN3	Transceiver output
A15	MOSYS1_CMDARX_N6	1.4-V PCML	AL3	Transceiver output
C14	MOSYS1_CMDARX_N7	1.4-V PCML	AJ3	Transceiver output
B21	MOSYS1_CMDARX_P0	1.4-V PCML	AY6	Transceiver output
D20	MOSYS1_CMDARX_P1	1.4-V PCML	AV6	Transceiver output
B19	MOSYS1_CMDARX_P2	1.4-V PCML	AU4	Transceiver output
D18	MOSYS1_CMDARX_P3	1.4-V PCML	AT6	Transceiver output
B17	MOSYS1_CMDARX_P4	1.4-V PCML	AR4	Transceiver output
D16	MOSYS1_CMDARX_P5	1.4-V PCML	AN4	Transceiver output
B15	MOSYS1_CMDARX_P6	1.4-V PCML	AL4	Transceiver output
D14	MOSYS1_CMDARX_P7	1.4-V PCML	AJ4	Transceiver output
A11	MOSYS1_CMDBRX_N0	1.4-V PCML	AG3	Transceiver output
C10	MOSYS1_CMDBRX_N1	1.4-V PCML	AE3	Transceiver output
A9	MOSYS1_CMDBRX_N2	1.4-V PCML	AC3	Transceiver output

Table 2–27. MoSys MSR576 Interface Pin Assignments, Signal Names and Functions (Part 2 of 5)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number	Description
C8	MOSYS1_CMDBRX_N3	1.4-V PCML	AA3	Transceiver output
A7	MOSYS1_CMDBRX_N4	1.4-V PCML	W3	Transceiver output
C6	MOSYS1_CMDBRX_N5	1.4-V PCML	U3	Transceiver output
A5	MOSYS1_CMDBRX_N6	1.4-V PCML	R3	Transceiver output
C4	MOSYS1_CMDBRX_N7	1.4-V PCML	N3	Transceiver output
B11	MOSYS1_CMDBRX_P0	1.4-V PCML	AG4	Transceiver output
D10	MOSYS1_CMDBRX_P1	1.4-V PCML	AE4	Transceiver output
B9	MOSYS1_CMDBRX_P2	1.4-V PCML	AC4	Transceiver output
D8	MOSYS1_CMDBRX_P3	1.4-V PCML	AA4	Transceiver output
B7	MOSYS1_CMDBRX_P4	1.4-V PCML	W4	Transceiver output
D6	MOSYS1_CMDBRX_P5	1.4-V PCML	U4	Transceiver output
B5	MOSYS1_CMDBRX_P6	1.4-V PCML	R4	Transceiver output
D4	MOSYS1_CMDBRX_P7	1.4-V PCML	N4	Transceiver output
T22	MOSYS1_CONFIGN	1.5-V CMOS	A16	Configuration enable
H22	MOSYS1_DMON_N0	1.5-V CMOS	—	Digital monitor
F3	MOSYS1_DMON_N1	1.5-V CMOS	—	Digital monitor
G22	MOSYS1_DMON_P0	1.5-V CMOS	—	Digital monitor
E3	MOSYS1_DMON_P1	1.5-V CMOS	—	Digital monitor
K22	MOSYS1_EVENTAN	1.5-V CMOS	C16	Error detect (CMDARX)
L21	MOSYS1_EVENTBN	1.5-V CMOS	H15	Error detect (CMDBRX)
AB21	MOSYS1_QATX_N0	1.4-V PCML	BB1	Transceiver input
Y20	MOSYS1_QATX_N1	1.4-V PCML	BA3	Transceiver input
AB19	MOSYS1_QATX_N2	1.4-V PCML	AY1	Transceiver input
Y18	MOSYS1_QATX_N3	1.4-V PCML	AW3	Transceiver input
AB17	MOSYS1_QATX_N4	1.4-V PCML	AV1	Transceiver input
Y16	MOSYS1_QATX_N5	1.4-V PCML	AT1	Transceiver input
AB15	MOSYS1_QATX_N6	1.4-V PCML	AP1	Transceiver input
Y14	MOSYS1_QATX_N7	1.4-V PCML	AM1	Transceiver input
AA21	MOSYS1_QATX_P0	1.4-V PCML	BB2	Transceiver input
W20	MOSYS1_QATX_P1	1.4-V PCML	BA4	Transceiver input
AA19	MOSYS1_QATX_P2	1.4-V PCML	AY2	Transceiver input
W18	MOSYS1_QATX_P3	1.4-V PCML	AW4	Transceiver input
AA17	MOSYS1_QATX_P4	1.4-V PCML	AV2	Transceiver input
W16	MOSYS1_QATX_P5	1.4-V PCML	AT2	Transceiver input
AA15	MOSYS1_QATX_P6	1.4-V PCML	AP2	Transceiver input
W14	MOSYS1_QATX_P7	1.4-V PCML	AM2	Transceiver input
AB11	MOSYS1_QBTX_N0	1.4-V PCML	AK1	Transceiver input
Y10	MOSYS1_QBTX_N1	1.4-V PCML	AH1	Transceiver input
AB9	MOSYS1_QBTX_N2	1.4-V PCML	AF1	Transceiver input

Table 2–27. MoSys MSR576 Interface Pin Assignments, Signal Names and Functions (Part 3 of 5)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number	Description
Y8	MOSYS1_QBTX_N3	1.4-V PCML	AD1	Transceiver input
AB7	MOSYS1_QBTX_N4	1.4-V PCML	AB1	Transceiver input
Y6	MOSYS1_QBTX_N5	1.4-V PCML	Y1	Transceiver input
AB5	MOSYS1_QBTX_N6	1.4-V PCML	V1	Transceiver input
Y4	MOSYS1_QBTX_N7	1.4-V PCML	T1	Transceiver input
AA11	MOSYS1_QBTX_P0	1.4-V PCML	AK2	Transceiver input
W10	MOSYS1_QBTX_P1	1.4-V PCML	AH2	Transceiver input
AA9	MOSYS1_QBTX_P2	1.4-V PCML	AF2	Transceiver input
W8	MOSYS1_QBTX_P3	1.4-V PCML	AD2	Transceiver input
AA7	MOSYS1_QBTX_P4	1.4-V PCML	AB2	Transceiver input
W6	MOSYS1_QBTX_P5	1.4-V PCML	Y2	Transceiver input
AA5	MOSYS1_QBTX_P6	1.4-V PCML	V2	Transceiver input
W4	MOSYS1_QBTX_P7	1.4-V PCML	T2	Transceiver input
F21	MOSYS1_RBIAS_0N	1.5-V CMOS	—	Calibration resistor
E21	MOSYS1_RBIAS_0P	1.5-V CMOS	—	Calibration resistor
F1	MOSYS1_RBIAS_1N	1.5-V CMOS	—	Calibration resistor
E1	MOSYS1_RBIAS_1P	1.5-V CMOS	—	Calibration resistor
M20	MOSYS1_READYN	1.5-V CMOS	K15	Device ready
Y22	MOSYS1_REFCLK_N	LVDS	—	Input reference clock
W22	MOSYS1_REFCLK_P	LVDS	—	Input reference clock
M22	MOSYS1_RESETN_IN	1.5-V CMOS	R15	Active low reset
P1	MOSYS1_SPI_SCLK	1.5-V CMOS	D17	SPI slave clock
T1	MOSYS1_SPI_SDI	1.5-V CMOS	C19	SPI data in or command
R2	MOSYS1_SPI_SDO	1.5-V CMOS	F19	SPI data out
U2	MOSYS1_SPI_SS	1.5-V CMOS	G19	SPI slave select, active low
H9	MOSYS1_VDD_KELVIN	1.0-V	—	VDD monitor point
H8	MOSYS1_VSS_KELVIN	GND	—	VSS monitor point
FPGA2 MoSys (U14)				
G20	MOSYS2_AMON_0	1.5-V CMOS	—	Analog monitor
B1	MOSYS2_AMON_1	1.5-V CMOS	—	Analog monitor
P22	MOSYS2_CLKDIVIDE	1.5-V CMOS	B16	REFCLK divider enable
A21	MOSYS2_CMDARX_N0	1.4-V PCML	AG3	Transceiver output
C20	MOSYS2_CMDARX_N1	1.4-V PCML	AE3	Transceiver output
A19	MOSYS2_CMDARX_N2	1.4-V PCML	AC3	Transceiver output
C18	MOSYS2_CMDARX_N3	1.4-V PCML	AA3	Transceiver output
A17	MOSYS2_CMDARX_N4	1.4-V PCML	W3	Transceiver output
C16	MOSYS2_CMDARX_N5	1.4-V PCML	U3	Transceiver output
A15	MOSYS2_CMDARX_N6	1.4-V PCML	R3	Transceiver output
C14	MOSYS2_CMDARX_N7	1.4-V PCML	N3	Transceiver output

Table 2–27. MoSys MSR576 Interface Pin Assignments, Signal Names and Functions (Part 4 of 5)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number	Description
B21	MOSYS2_CMDARX_P0	1.4-V PCML	AG4	Transceiver output
D20	MOSYS2_CMDARX_P1	1.4-V PCML	AE4	Transceiver output
B19	MOSYS2_CMDARX_P2	1.4-V PCML	AC4	Transceiver output
D18	MOSYS2_CMDARX_P3	1.4-V PCML	AA4	Transceiver output
B17	MOSYS2_CMDARX_P4	1.4-V PCML	W4	Transceiver output
D16	MOSYS2_CMDARX_P5	1.4-V PCML	U4	Transceiver output
B15	MOSYS2_CMDARX_P6	1.4-V PCML	R4	Transceiver output
D14	MOSYS2_CMDARX_P7	1.4-V PCML	N4	Transceiver output
A11	MOSYS2_CMDBRX_N0	1.4-V PCML	L3	Transceiver output
C10	MOSYS2_CMDBRX_N1	1.4-V PCML	J3	Transceiver output
A9	MOSYS2_CMDBRX_N2	1.4-V PCML	K5	Transceiver output
C8	MOSYS2_CMDBRX_N3	1.4-V PCML	H5	Transceiver output
A7	MOSYS2_CMDBRX_N4	1.4-V PCML	G3	Transceiver output
C6	MOSYS2_CMDBRX_N5	1.4-V PCML	F5	Transceiver output
A5	MOSYS2_CMDBRX_N6	1.4-V PCML	E3	Transceiver output
C4	MOSYS2_CMDBRX_N7	1.4-V PCML	D5	Transceiver output
B11	MOSYS2_CMDBRX_P0	1.4-V PCML	L4	Transceiver output
D10	MOSYS2_CMDBRX_P1	1.4-V PCML	J4	Transceiver output
B9	MOSYS2_CMDBRX_P2	1.4-V PCML	K6	Transceiver output
D8	MOSYS2_CMDBRX_P3	1.4-V PCML	H6	Transceiver output
B7	MOSYS2_CMDBRX_P4	1.4-V PCML	G4	Transceiver output
D6	MOSYS2_CMDBRX_P5	1.4-V PCML	F6	Transceiver output
B5	MOSYS2_CMDBRX_P6	1.4-V PCML	E4	Transceiver output
D4	MOSYS2_CMDBRX_P7	1.4-V PCML	D6	Transceiver output
T22	MOSYS2_CONFIGN	1.5-V CMOS	A16	Configuration enable
H22	MOSYS2_DMON_N0	1.5-V CMOS	—	Digital monitor
F3	MOSYS2_DMON_N1	1.5-V CMOS	—	Digital monitor
G22	MOSYS2_DMON_P0	1.5-V CMOS	—	Digital monitor
E3	MOSYS2_DMON_P1	1.5-V CMOS	—	Digital monitor
K22	MOSYS2_EVENTAN	1.5-V CMOS	C16	Error detect (CMDARX)
L21	MOSYS2_EVENTBN	1.5-V CMOS	H15	Error detect (CMDBRX)
AB21	MOSYS2_QATX_N0	1.4-V PCML	AK1	Transceiver input
Y20	MOSYS2_QATX_N1	1.4-V PCML	AH1	Transceiver input
AB19	MOSYS2_QATX_N2	1.4-V PCML	AF1	Transceiver input
Y18	MOSYS2_QATX_N3	1.4-V PCML	AD1	Transceiver input
AB17	MOSYS2_QATX_N4	1.4-V PCML	AB1	Transceiver input
Y16	MOSYS2_QATX_N5	1.4-V PCML	Y1	Transceiver input
AB15	MOSYS2_QATX_N6	1.4-V PCML	V1	Transceiver input
Y14	MOSYS2_QATX_N7	1.4-V PCML	T1	Transceiver input

Table 2–27. MoSys MSR576 Interface Pin Assignments, Signal Names and Functions (Part 5 of 5)

Board Reference	Schematic Signal Name	I/O Standard	Stratix V GX FPGA Device Pin Number	Description
AA21	MOSYS2_QATX_P0	1.4-V PCML	AK2	Transceiver input
W20	MOSYS2_QATX_P1	1.4-V PCML	AH2	Transceiver input
AA19	MOSYS2_QATX_P2	1.4-V PCML	AF2	Transceiver input
W18	MOSYS2_QATX_P3	1.4-V PCML	AD2	Transceiver input
AA17	MOSYS2_QATX_P4	1.4-V PCML	AB2	Transceiver input
W16	MOSYS2_QATX_P5	1.4-V PCML	Y2	Transceiver input
AA15	MOSYS2_QATX_P6	1.4-V PCML	V2	Transceiver input
W14	MOSYS2_QATX_P7	1.4-V PCML	T2	Transceiver input
AB11	MOSYS2_QBTX_N0	1.4-V PCML	P1	Transceiver input
Y10	MOSYS2_QBTX_N1	1.4-V PCML	M1	Transceiver input
AB9	MOSYS2_QBTX_N2	1.4-V PCML	K1	Transceiver input
Y8	MOSYS2_QBTX_N3	1.4-V PCML	H1	Transceiver input
AB7	MOSYS2_QBTX_N4	1.4-V PCML	F1	Transceiver input
Y6	MOSYS2_QBTX_N5	1.4-V PCML	B1	Transceiver input
AB5	MOSYS2_QBTX_N6	1.4-V PCML	D1	Transceiver input
Y4	MOSYS2_QBTX_N7	1.4-V PCML	C3	Transceiver input
AA11	MOSYS2_QBTX_P0	1.4-V PCML	P2	Transceiver input
W10	MOSYS2_QBTX_P1	1.4-V PCML	M2	Transceiver input
AA9	MOSYS2_QBTX_P2	1.4-V PCML	K2	Transceiver input
W8	MOSYS2_QBTX_P3	1.4-V PCML	H2	Transceiver input
AA7	MOSYS2_QBTX_P4	1.4-V PCML	F2	Transceiver input
W6	MOSYS2_QBTX_P5	1.4-V PCML	B2	Transceiver input
AA5	MOSYS2_QBTX_P6	1.4-V PCML	D2	Transceiver input
W4	MOSYS2_QBTX_P7	1.4-V PCML	C4	Transceiver input
F21	MOSYS2_RBIAS_0N	1.5-V CMOS	—	Calibration resistor
E21	MOSYS2_RBIAS_0P	1.5-V CMOS	—	Calibration resistor
F1	MOSYS2_RBIAS_1N	1.5-V CMOS	—	Calibration resistor
E1	MOSYS2_RBIAS_1P	1.5-V CMOS	—	Calibration resistor
M20	MOSYS2_READYN	1.5-V CMOS	K15	Device ready
Y22	MOSYS2_REFCLK_N	LVDS	—	Input reference clock
W22	MOSYS2_REFCLK_P	LVDS	—	Input reference clock
M22	MOSYS2_RESETN_IN	1.5-V CMOS	R15	Active low reset
P1	MOSYS2_SPI_SCLK	1.5-V CMOS	D17	SPI slave clock
T1	MOSYS2_SPI_SDI	1.5-V CMOS	C19	SPI data in
R2	MOSYS2_SPI_SDO	1.5-V CMOS	F19	SPI data out
U2	MOSYS2_SPI_SS	1.5-V CMOS	G19	SPI slave select
H9	MOSYS2_VDD_KELVIN	1.0-V	—	VDD monitor point
H8	MOSYS2_VSS_KELVIN	GND	—	VSS monitor point

Flash

The development board supports a 1-Gb CFI-compatible synchronous flash device for non-volatile storage of FPGA configuration data, board information, and test application data.

The interface has a 16-bit data bus and connects to the MAX V System Controller. The interface can sustain burst read operations at up to 52 MHz for a throughput of 832 Mbps per device. The write performance is 270 µs for a single word and 310 µs for a 32-word buffer. The erase time is 800 ms for a 128 K parameter block.

Table 2–28 lists the flash pin assignments, signal names, and functions.

Table 2–28. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference (U86)	Schematic Signal Name	I/O Standard	Description
A1	FLASH_A1	1.8-V	Address bus
B1	FLASH_A2	1.8-V	Address bus
C1	FLASH_A3	1.8-V	Address bus
D1	FLASH_A4	1.8-V	Address bus
D2	FLASH_A5	1.8-V	Address bus
A2	FLASH_A6	1.8-V	Address bus
C2	FLASH_A7	1.8-V	Address bus
A3	FLASH_A8	1.8-V	Address bus
B3	FLASH_A9	1.8-V	Address bus
C3	FLASH_A10	1.8-V	Address bus
D3	FLASH_A11	1.8-V	Address bus
C4	FLASH_A12	1.8-V	Address bus
A5	FLASH_A13	1.8-V	Address bus
B5	FLASH_A14	1.8-V	Address bus
C5	FLASH_A15	1.8-V	Address bus
D7	FLASH_A16	1.8-V	Address bus
D8	FLASH_A17	1.8-V	Address bus
A7	FLASH_A18	1.8-V	Address bus
B7	FLASH_A19	1.8-V	Address bus
C7	FLASH_A20	1.8-V	Address bus
C8	FLASH_A21	1.8-V	Address bus
A8	FLASH_A22	1.8-V	Address bus
G1	FLASH_A23	1.8-V	Address bus
H8	FLASH_A24	1.8-V	Address bus
B6	FLASH_A25	1.8-V	Address bus
B8	FLASH_A26	1.8-V	Address bus
F6	FLASH_ADVN	1.8-V	Address valid
B4	FLASH_CEN	1.8-V	Chip enable
E6	FLASH_CLK	1.8-V	Clock

Table 2–28. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference (U86)	Schematic Signal Name	I/O Standard	Description
F2	FLASH_D0	1.8-V	Data bus
E2	FLASH_D1	1.8-V	Data bus
G3	FLASH_D2	1.8-V	Data bus
E4	FLASH_D3	1.8-V	Data bus
E5	FLASH_D4	1.8-V	Data bus
G5	FLASH_D5	1.8-V	Data bus
G6	FLASH_D6	1.8-V	Data bus
H7	FLASH_D7	1.8-V	Data bus
E1	FLASH_D8	1.8-V	Data bus
E3	FLASH_D9	1.8-V	Data bus
F3	FLASH_D10	1.8-V	Data bus
F4	FLASH_D11	1.8-V	Data bus
F5	FLASH_D12	1.8-V	Data bus
H5	FLASH_D13	1.8-V	Data bus
G7	FLASH_D14	1.8-V	Data bus
E7	FLASH_D15	1.8-V	Data bus
F8	FLASH_OEN	1.8-V	Output enable
F7	FLASH_RDYBSYN	1.8-V	Ready
D4	FLASH_RESETN	1.8-V	Reset
G8	FLASH_WEN	1.8-V	Write enable
C6	FLASH_WPN	1.8-V	Write protect

Power Supply

The development board's power is provided through a laptop style DC power input or through the PCI Express edge connector. The DC voltage is stepped down to the various power rails used by the components on the board or components installed into the HSMC connectors. A PCI Express compliant 2x4 ATX power connector is also available in addition to the DC power input or the PCI Express edge connector power. The 2x4 ATX power supply is 12 V with 12.5 A, providing up to an additional 150 W to the board.

An on-board multi-channel analog-to-digital converter (ADC) measures both the voltage and current for several specific board rails. The power utilization is displayed in a GUI that graphs power consumption versus time.

Table 2–29 lists the maximum allowed draws of the power input.

Table 2–29. Power Input Maximum Allowed Draws

Source	Voltage (V)	Current (A)	Wattage (W)
25 W PCI Express edge connector	3.3	—	—
	12.0	—	—
75 W PCI Express edge connector	3.3	3.0	9.0
	12.0	5.5	66.0
Laptop Supply—DC input (1)	15.0	8.0	120.0
2x4 PCI Express ATX connector	12.0	12.5	150.0

Note to Table 2–29:

(1) The minimum and maximum voltage allowed for the DC input is 12 V and 16 V respectively.

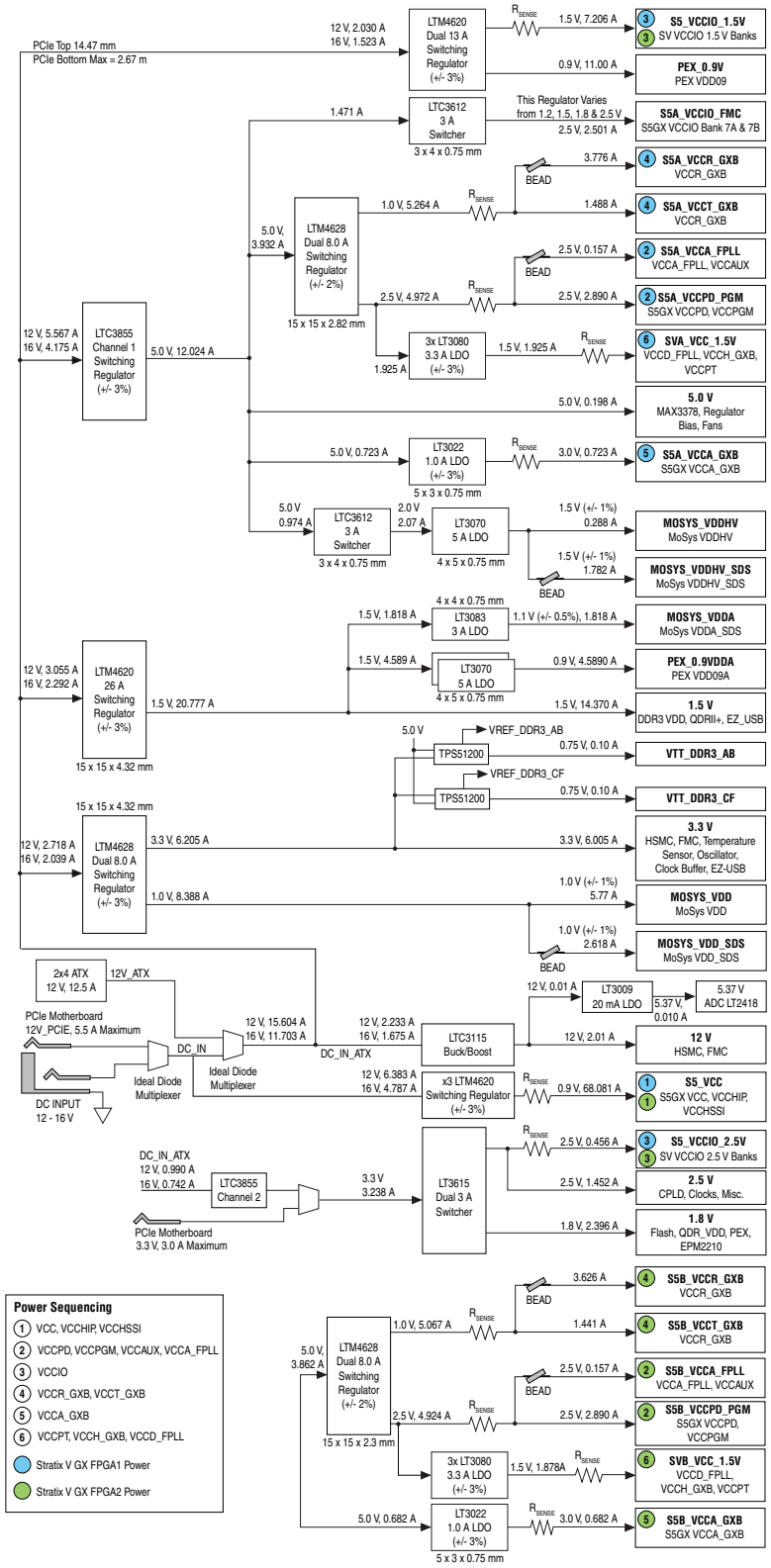
Power Distribution System

The power tree minimizes power board space for the PCI Express 225 W High Power board requirements and gives the maximum power under 5.5 A for a 12 V PCI Express input and 3.0 A for a 3.3 V PCI Express rail. As per the 225 W High Power specification, a 2x4 ATX connector is available to supply 12.5 A for an additional 12 V power rail to the board.

The switching regulators are assumed to have 85% of efficiency. Regulator inefficiencies and sharing are reflected in the currents shown, which are conservative absolute maximum levels.

Figure 2–8 shows the power distribution system on the development board.

Figure 2–8. Power Distribution System



Power Measurement

There are 16 power supply rails which have on-board voltage, current, and wattage sense capabilities. The 8-channel differential 24-bit ADC device and rails are split from the primary supply plane by a low-value sense resistor for the ADC to measure voltage and current. A serial peripheral interface (SPI) bus connects the ADC device to the MAX V CPLD System Controller.

Figure 2–9 shows the block diagram for the power measurement circuitry.

Figure 2–9. Power Measurement Circuit

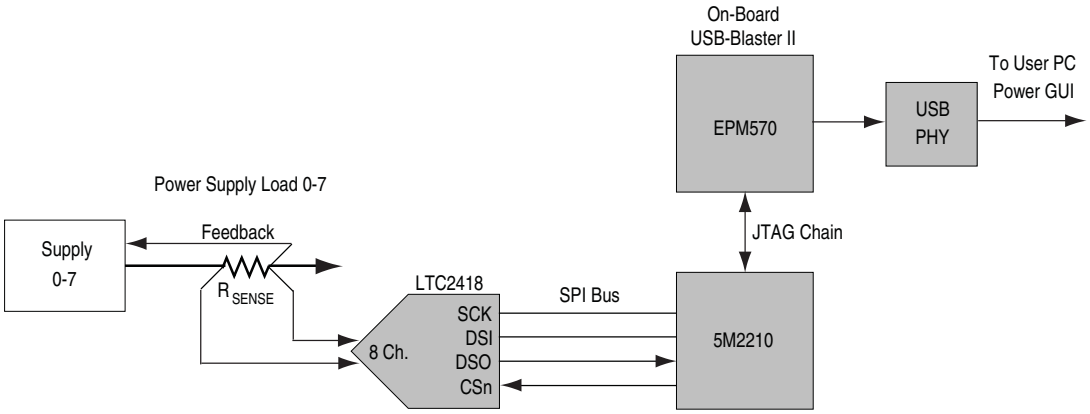


Table 2–30 lists the targeted rails. The schematic signal name specifies the name of the rail being measured and the device pin specifies the devices attached to the rail. If no subnet is named, the power is the total output power for that voltage.

Table 2–30. Power Rail Measurements Based on the GUI Selection

Number	Schematic Signal Name	Voltage (V)	Device Pin	Description
0	S5A_VCCPD_PGM	2.50	VCCPD	FPGA1 I/O pre-drivers
			VCCPGM	FPGA1 configuration I/O
1	S5_VCCIO_1.5V	1.50	VCCIO3[B:E]	FPGA1 and FPGA2 VCCIO banks
			VCCIO4[B:E]	FPGA1 and FPGA2 VCCIO banks
			VCCIO7[C:E]	FPGA1 and FPGA2 VCCIO banks
			VCCIO8[A:E]	FPGA1 and FPGA2 VCCIO banks
2	S5B_VCCR_GXB	1.00	VCCR_GXB	FPGA2 XCVR analog receive
3	S5_VCC	0.90	VCC	FPGA1 and FPGA2 core and periphery power
			VCCHIP_[L,R]	FPGA1 and FPGA2 PCI Express Hard IP digital power
			VCCHSSI_[L,R]	FPGA1 and FPGA2 XVCR PCS power
4	S5B_VCCPD_PGM	2.50	VCCPD	FPGA2 I/O pre-drivers
			VCCPGM	FPGA2 configuration I/O
5	S5_VCCIO_2.5V	2.50	VCCIO4A	FPGA1 and FPGA2 VCCIO bank 4A
6	S5A_VCCR_GXB	1.00	VCCR_GXB	FPGA1 XCVR analog receive
7	—	—	—	—

Temperature Sense

Temperature monitoring for both Stratix V GX FPGA dies is achieved with a MAX1619 temperature sense device. The MAX1619 device connects to the MAX V CPLD System Controller by a 2-wire SMB interface. The MAX1619 device is located at address 0x1 for FPGA1 and address 0x2 for FPGA2.

The FPGA1_OVERTEMP and TSENSE_ALERTn_1 signals are driven by the MAX1619 temperature sense device based on a programmable threshold temperature for FPGA1. The FPGA1_OVERTEMP signal is driven to the MAX V CPLD System Controller to control FPGA1 fan speed. The FPGA2_OVERTEMP and TSENSE_ALERTn_2 signals are driven by the MAX1619 temperature sense device based on a programmable threshold temperature for FPGA2. The FPGA2_OVERTEMP signal is driven to the MAX V CPLD System Controller to control FPGA2 fan speed.

The MAX V CPLD System Controller can control fan speed for each FPGA based on a register setting and can also override the MAX1619 device. For more information about this control, refer to the MAX V CPLD System Controller source code found in the development board installation directory *<install dir>*\stratixVGX_5sgxea7nf45_as\examples\max5.

For more information on the development board installation directory, refer to the *Stratix V Advanced Systems Development Kit User Guide*.

The remote sense routes to the FPGA's diode pins to measure the voltage drop. For very accurate temperature readings, the I/O adjacent to the FPGA diode sense pins must be halted.

Table 2–31 lists the temperature sense interface pin assignments, signal names, and functions.

Table 2–31. Temperature Sense Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	I/O Standard	MAX V CPLD System Controller Pin Number	Stratix V GX FPGA Device Pin Number	Description
FPGA1 MAX1619 (U102)					
14	SENSE_SMB_CLK	2.5-V	E7	—	SMB clock
12	SENSE_SMB_DATA	2.5-V	E6	—	SMB data
11	TSENSE_ALERTn_1	2.5-V	D8	—	Programmable over temperature alert
9	FPGA1_OVERTEMPn	2.5-V	D7	—	Fan enable
3	FPGA1_TEMPDIODE_P	2.5-V	—	P6	Current source and remote diode input
4	FPGA1_TEMPDIODE_N	2.5-V	—	P7	Remote diode input
FPGA2 MAX1619 (U103)					
14	SENSE_SMB_CLK	2.5-V	E7	—	SMB clock
12	SENSE_SMB_DATA	2.5-V	E6	—	SMB data
11	TSENSE_ALERTn_2	2.5-V	B5	—	Programmable over temperature alert
9	FPGA2_OVERTEMPn	2.5-V	E10	—	Fan enable
3	FPGA2_TEMPDIODE_P	2.5-V	—	P6	Current source and remote diode input
4	FPGA2_TEMPDIODE_N	2.5-V	—	P7	Remote diode input

3. Board Components Reference

This chapter lists the component reference and manufacturing information of all the components on the Stratix V Advanced Systems development board.

Table 3–1. Component Reference and Manufacturing Information

Board Reference	Component	Manufacturer	Manufacturing Part Number	Manufacturer Website
U29, U35	FPGA, Stratix V GX F1932, 622K LEs, leadfree	Altera Corporation	5SGXEA7N2F45C2N	www.altera.com
U73	MAX V CPLD 2210 LE 256-pin FBGA LF 1.8V VCCINT	Altera Corporation	5M2210ZF256C4N	www.altera.com
U77	MAX II CPLD 570 LE 100-pin FBGA	Altera Corporation	EPM570F100C5N	www.altera.com
U63	High-Speed USB peripheral controller	Cypress	CY7C68013A-56LTXCx	www.cypress.com
D1-D5, D10-D13, D15, D16, D21, D34-D36	Green LEDs, 0805 SMD	Lumex Inc.	SML-LXT0805GW-TR	www.lumex.com
D14, D26, D37	Red LED, 0805 SMD	Lumex Inc.	SML-LXT0805IW-TR	www.lumex.com
D27	Blue LED	Lumex Inc.	SML-LX0805USBC-TR	www.lumex.com
D6-D9, D17-D20, D22-D25, D28-D31	Bi-color LEDs—green, 0805 SMD/ red, 0606 SMT	Lite-On, Inc.	LTST-C195GEKT	www.us.liteon.com
SW5-SW8	Four-Position DIP switch	C & K Components	TDA04H0SB1	www.ck-components.com
SW4	Six-Position DIP switch	C & K Components	TDA06H0SB1	www.ck-components.com
SW1, SW3	Eight-Position DIP switch	C & K Components	TDA08H0SB1	www.ck-components.com
S1-S11	Push button	Dawning Precision Co., Ltd.	TS-A02SA-2-S100	www.dawning2.com.tw
SW2	Slide switch	E-switch	EG2207	www.e-switch.com
X1	125.00 MHz LVDS crystal oscillator	Epson	EG-2121CA 125.0000M-LGPNL3	www.eea.epson.com
X2	50 MHz 1.8-V oscillator	ECS, Inc.	ECS-3518-500-B-xx	www.ecsxtal.com
X3	100 MHz 2.5-V CMOS oscillator	ECS, Inc.	ECS-3525-1000-B-TR	www.ecsxtal.com
U59	One differential to four LVDS output clock buffer	Silicon Labs	Si5330B-A00205-GM	www.silabs.com
U82, U100	Programmable quad clock, I²C 0x78, defaults LVDS 100 MHz, LVDS 100 MHz, 1.8V (A ONLY) 100 MHz, LVDS 100 MHz	Silicon Labs	Si5338A-A01449-GM	www.silabs.com

Table 3–1. Component Reference and Manufacturing Information

Board Reference	Component	Manufacturer	Manufacturing Part Number	Manufacturer Website
U91	Programmable quad clock, I²C 0x72, defaults LVDS 100 MHz, 644.53125 MHz, 644.53125 MHz, 100 MHz	Silicon Labs	Si5338A-A01392-GM	www.silabs.com
U95	Programmable quad clock, I²C 0x74, defaults LVDS 100 MHz, 706.25 MHz, 206.25 MHz, 206.25 MHz	Silicon Labs	Si5338A-A01603-GM	www.silabs.com
U53	Programmable quad clock, I²C 0x76, defaults LVDS 625 MHz, 206.25 MHz, 625 MHz, 206.25 MHz	Silicon Labs	Si5338A-A01604-GM	www.silabs.com
U50	Two differential to 6 LVDS output clock buffer	IDT	5T9306NLGI	www.idt.com
U62	1 to 3 single-ended clock buffer	Silicon Labs	SL18860DC	www.silabs.com
U85	PCI Express Gen1, Gen2, Gen3 quad fan out buffer	Silicon Labs	Si53154-A01AGMx	www.silabs.com
J10	2x4, 4.20-mm pitch header, dual row, right angle	Molex	50-34-8571	www.molex.com
J8	FMC pitch socket array assembly connector	Samtec	ASP-134486-01	www.samtec.com
J1	HSMC, custom version of QSH-DP family high-speed socket	Samtec	ASP-122953-01	www.samtec.com
U19, U57, U36, U81, U30, U34, U80, U72, U21, U58, U68, U27, U32, U75, U88, U39, U92,U43, U33, U78, U17, U24, U55, U64	16M × 16-bit × 8 banks DDR3 SDRAM	Micron	MT41J128M16JT-093	www.micron.com
U12, U52, U41, U90, U22, U61, U40, U89	2M × 18, 550 MHZ QDRII+ SRAM	Cypress	CY7C2263KV18-550BZXI	www.cypress.com
U4, U14	2M × 72, 576-Mb MoSys MSR576 SRAM	MoSys	MSR576TE8888AB-103	www.mosys.com
U86	1-Gb synchronous flash	Numonyx	PC28F00AP30BF	www.numonyx.com
U48, U93	256-Mb, multi I/O serial flash, 3 V	Micron	N25Q256A13EF840x	www.micron.com
U99	8-channel differential 24-bit ADC	Linear Technology	LTC2418CGN#PBF	www.linear.com
U102, U103	Temperature sense, remote and local, programmable alert.	Maxim	MAX1619MEE+T	www.maxim-ic.com

Statement of China-RoHS Compliance

Table 3–2 lists hazardous substances included with the kit.

Table 3–2. Table of Hazardous Substances' Name and Concentration *Notes (1), (2)*

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Stratix V Advanced Systems development board	X*	0	0	0	0	0
15 V power supply	0	0	0	0	0	0
Type USB-A to mini USB-B cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 3–2:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

This chapter provides additional information about the board, document, and Altera.

Board Revision History

The following table lists the versions of all releases of the Stratix V Advanced Systems development board.

Release Date	Version	Description
January 2013	Production silicon	Initial release.

Document Revision History

The following table lists the revision history for this document.

Date	Version	Changes
January 2014	1.1	Updated the I/O standard for SVA_CLK_50 and SVB_CLK_50 in Table 2–12.
January 2013	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.
	The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.